SC6600D Device Specifications

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Table of Contents

1 Overview 9
1.1 SC6600D Features 9
1.2 Applications 10
1.3 General Description 10
1.4 Block Diagram 12
2 Pin Information 13
2.1 Pin Type Description 13
2.2 Pin List by Pin Numbers 13
2.3 Pin List by Functions 17
2.4 Package Pin Map 23
3 Electrical Specifications 24
3.1 DC Specifications 24
3.1.1 Absolute Maximum Ratings 24
3.1.2 Recommended Operating Conditions 24
3.1.3 Thermal Characteristics 24
3.1.4 DC Characteristics 24
3.2 AC Specifications 25
3.2.1 Master Clock MCLKI Timing 26
3.2.2 Three-Wire Serial Interface Timing 27
3.2.3 JTAG Timing 29
3.3 Performance Specifications 29
3.3.1 Baseband 30
3.3.1.1 Baseband Transmit Path 30
3.3.1.2 Baseband Receive Path 30
3.3.2 Voice Band 31
3.3.2.1 Voice Band Uplink ADC 31
3.3.2.2 Voice Band Downlink DAC 31
3.3.3 Phase-Locked Loop (PLL) 32
3.3.4 Auxiliary Digital-to-Analog Converters 32
3.3.4.1 Automatic Frequency Control (AFC) 32
3.3.4.2 RF Power Ramping Control DAC 33
3.3.5 Auxiliary Analog-to-Digital Converter 33
3.3.6 LDO 33
4 Functional Description 35
4.1 MCU Core and Internal Memories 35
4.1.1 MCU Core 35
4.1.2 MCU Internal SRAM 35
4.1.3 MCU Internal ROM 35
4.1.4 MCU Boot 35
4.1.5 MCU Memory Address Map 36
4.2 MCU External Memory Controller 36
4.2.1 MCU External Memory Interface 36
4.2.2 External Memory Timing for a Single Access 36
4.2.3 External Memory Timing for a Burst Access 36
4.2.4 SDRAM Support 36
4.2.5 NAND Flash Support 36
4.2.6 Memory Bus Sharing 36
4.2.7 External Memory Control Registers 36
4.3 MCU Memory Remap and MCU Stop 36
4.3.1 MCU Stop 36
4.3.2 MCU Memory Remap 36
4.3.3 Remap and Pause Control Registers 36
4.4 MCU Bus DMA 36
4.4.1 MCU Bus DMA Control Registers 36
4.5 MCU Bus Monitor 36

This document contains information on a product under development.
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4.5.1 Bus Monitor Control Registers 36
4.6 MCU Interrupt Controller 36
4.6.1 Interrupt Control Registers 36
4.7 MCU Timers 36
4.7.1 General-Purpose Timers 36
4.7.1.1 Timer Control Registers 36
4.7.2 32-bit System Counter 36
4.7.2.1 32-bit System Counter Registers 36
4.7.3 Watchdog Timer 36
4.7.3.1 Watchdog Timer Registers (0x8900_3000) 36
4.8 MCU Peripherals 36
4.8.1 UART Controller 36
4.8.1.1 Overview 36
4.8.1.2 Functional Description 36
4.8.1.3 6-Wire UART Interface 36
4.8.1.4 2-Wire UART Interface 36
4.8.1.5 UART Registers 36
4.8.2 IrDA Interface 36
4.8.2.1 IrDA Controller 36
4.8.2.2 IrDA Control Registers 36
4.8.3 SPI Interface 36
4.8.3.1 SPI Registers 36
4.8.4 SIM Card Interface 36
4.8.4.1 SIM Functional Description 36
4.8.4.2 SIM Clock and Baud Rate Control 36
4.8.4.3 SIM Activation and Deactivation 36
4.8.4.4 Activation and Deactivation 36
4.8.4.5 SIM Data Tx and Rx 36
4.8.4.6 Rx/Tx Control 36
4.8.4.7 Retransmission 36
4.8.4.8 SIM Power Supply 36
4.8.4.9 Unresponsive Card Detection 36
4.8.4.10 SIM Interface Watchdog 36
4.8.4.11 SIM Interface Separate Timing Control 36
4.8.4.12 SIM Card Interface Registers 36
4.8.5 Two-Wire Serial Interface 36
4.8.5.1 Features 36
4.8.5.2 Two-Wire Interface Connection 36
4.8.5.3 Clock Divisor 0 & 1 Registers 36
4.8.5.4 Operation 36
4.8.5.5 Arbitration Procedure 36
4.8.5.6 Programming Examples 36
4.8.5.7 Two-Wire Serial Port Control Registers 36
4.8.6 Keypad Interface 36
4.8.6.1 Non-Time-Out Mode 36
4.8.6.2 Time-Out Mode 36
4.8.6.3 Sleep Mode 36
4.8.6.4 Keypad Registers 36
4.8.7 Pulse Width Modulation Outputs 36
4.8.7.1 PWM Registers 36
4.8.8 MCU GPIO 36
4.8.8.1 MCU GPIO Control Registers 36
4.8.9 Auxiliary Analog-to-Digital Converter (ADC) 36
4.8.9.1 Auxiliary ADC control registers 36
4.9 Real Time Clock 36
4.9.1 Real Timer Clock Registers 36
4.10 GEA Accelerator 36
4.10.1 GPRS Encryption Algorithm (GEA) 36
4.10.2 GEA Accelerator Control 36
4.11 MCU Global Registers 36

This document contains information on a product under development.
Spreadtrum reserves the right to change or discontinue this product without notice.

4.12 Chip Pin Control 36
4.12.1 Pin Function Selection 36
4.12.2 Pad Driving Strength 36
4.12.3 Pad Weak Pull-Up 36
4.12.4 Chip Pin Control Registers 36
4.13 Chip ID Register 36
4.14 JTAG Interface 36
4.15 Charger Control 36
4.15.1 Monitor of Charging Current and Battery Voltage 36
4.15.2 Charging Current 36
4.15.3 Recharge Control 36
4.15.4 Charger Control Registers 36
5 Package Outline 36

This document contains information on a product under development.
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List of Figures

Figure 1: SC6600D chip-level functional block diagram. 12
Figure 2: Pin configuration. 23
Figure 3: MCLKI Timing Parameters. 26
Figure 4: Three-wire serial interface timing parameters (mode 1). 27
Figure 5: Three-wire serial interface timing parameters (mode 2). 28
Figure 6: JTAG Interface Timing 29
Figure 7: MCU external memory timing for a single access. 36
Figure 8: MCU external memory access for a burst access. 36
Figure 9: MCU interrupt controller. 36
Figure 10: Two-wire serial interface protocol. 36
Figure 11: Clock synchronization on the two-wire serial bus. 36
Figure 12: Two-wire serial port write example. 36
Figure 13: Two-wire serial port read example. 36
Figure 14: Keypad connection. 36
Figure 15: PWM module block diagram. 36
Figure 16: PWM module functional block diagram. 36
Figure 17: Auxiliary ADC. 36
Figure 18: SC6600D charger connection. 36

This document contains information on a product under development.
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List of Tables

Table 1: I/O pin type description. 13
Table 2: List of SC6600D pins by pad numbers. 13
Table 3: List of SC6600 pins by functions. 17
Table 4: Absolute maximum ratings of SC6600D. 24
Table 5: Recommended operating conditions. 24
Table 6: Thermal characteristics. 24
Table 7: DC characteristics. 25
Table 8: AC characteristics. 26
Table 9: MCLKI Timing Parameters. 26
Table 10: Three-wire serial interface timing parameters. 29
Table 11: JTAG Interface Timing. 29
Table 12: Performance of the baseband transmit path. 30
Table 13: Performance of the baseband receive path. 31
Table 14: Performance of the voice band ADC. 31
Table 15: Performance of the voice band DAC. 31
Table 16: Performance of the phase-locked loop (PLL only). 32
Table 17: Performance of the AFC DAC. 32
Table 18: Performance of the RF power ramping control DAC. 33
Table 19: Performance of the auxiliary ADC. 33
Table 20: Performance of the integrated LDO regulators. 33
Table 21: List of MCU boot options. 36
Table 22: SC6600D MCU memory address map after reset. 36
Table 23: External memory control registers (base address: 0x2000_0000). 36
Table 24: Remap and pause control registers (base address: 0x8200_0000). 36
Table 25: DMA control registers (base address: 0x2010_0000). 36
Table 26: Bus monitor control registers (base address: 0x2000_0000). 36
Table 27: MCU Interrupt control registers (base address: 0x8000_0000). 36
Table 28: Timer control registers (base address: 0x8100_0000). 36
Table 29: 32-bit system counter registers (base address: 0x8700_0000). 36
Table 30: Watchdog timer registers (base address: 0x8900_0300). 36
Table 31: List of UART pins. 36
Table 32: UART control registers. 36
Table 33: IrDA control registers. 36
Table 34: Organization of the serial ports. 36
Table 35: Pin mapping for the serial ports. 36
Table 36: SPI control registers (base address: 0x8300_0000, 0xBE00). 36
Table 37: SIM clock control. 36
Table 38: SIM card interface registers (base address: 0x8500_0000). 36
Table 39: Two-wire serial port control registers (base address: 0x8600_0000). 36
Table 40: Keypad control registers (base address: 0x8700_0000). 36
Table 41: PWM control registers (base address: 0x8800_0000). 36
Table 42: MCU GPIO control registers (base address: 0x8A00_0000). 36
Table 43: Auxiliary ADC control registers (base address: 0x8B00_0000). 36
Table 44: Real time clock registers (base address: 0x8900_0000). 36
Table 45: GEA accelerator control registers (base address: 0x8D00_0000). 36
Table 46: MCU global registers (base address: 0x8B00_0000). 36
Table 47: SC6600D I/O Driving strength control. 36
Table 48: Chip pin control registers (base address: 0x8C00_0000). 36
Table 49: Chip ID register (base address: 0xFFFF_FFFC). 36
Table 50: Charger control registers (base address: 0x8A00_0180). 36

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1 Overview

1.1 SC6600D Features

SC6600D is a second-generation chip in the SC6600 series of Spreadtrum GSM/GPRS ASIC solutions. It contains all of the SC6600B features (with improvements), including:

- Low power and high-performance device in a 0.18 μm mixed signal CMOS technology.
  - External supply voltages: battery 3.6 V (typical), backup battery (optional) 3.0 V (typical) and RTC power supply 1.8 V (typical).
  - Internal supply voltages: analog 2.8 V (typical), digital I/O 3.0 V or 1.8 V (typical) and digital core 1.8 V (typical).
- 12 x 12 mm^2 180-ball 0.8 ball pitch LFBGA package.
- Compatible with GSM/GPRS Release 1999, DCS1800 and PCS1900 recommendations.
- Dedicated GSM/GPRS signal processing engine for equalization, channel encoding/decoding for all traffic and control channels, GMSK modulation and encryption/decryption (A5/1 and A5/2, GEA 1 and GEA 2 algorithms).
- GSM system timing:
  - Low swing 13 MHz master clock input.
  - Programmable TDMA timing with 1/4 bit resolution.
  - Time tracking in power saving mode.
- Embedded microcontroller (MCU) for protocol stack and peripheral control:
  - ARM7TDMI®, 32-bit RISC processor.
  - Up to 64 k byte on-chip RAM.
  - 40 k byte on-chip ROM.
  - External memory interface.
  - JTAG for test and In-Circuit Emulation.
- Embedded DSP core for all GSM/GPRS specific signal processing tasks:
  - TeakLite®, 16-bit fixed point DSP core.
  - Up to 80 k byte on-chip program RAM.
  - 80 k byte on-chip program ROM.
  - 32 k byte on-chip data RAM.
  - 32 k byte on-chip data ROM.
- Complete in-phase and quadrature (I/Q) component interface between the Digital Signal Processor (DSP) and RF module.
- Dedicated RF serial control interface and parallel control signals.
- Complete voice band codec:
  - Audio signal conversion between microphone/earphone and DSP.
  - Second set converters for auxiliary microphone/speaker.
  - Support of the Digital Audio Interface (DAI).
- Five auxiliary analog inputs to a 10-bit analog-to-digital converter (ADC) for measurement purposes.
- Three auxiliary analog outputs from digital-to-analog converters (DAC) for control purposes (AFC, RF power ramping control and one spare).
- SIM card interface.
- PCMCIA interface.
- Serial/parallel interfaces:
  - Three UART, up to 460 k baud rate.
  - IrDA.
  - Two-wire serial interface.
  - Three-wire serial interface.
- On-chip PLL for programmable microcontroller and DSP clocks.
- Real time clock (RTC) and alarm running on a 32.768 kHz crystal.
- Power management with LDO for on-chip as well as off-chip circuitry.

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In addition, SC6600D provides the following new features.

- Improved voice band.
  - Stereo audio output.
  - Integrated microphone bias.
- Battery charger.
- 1.8 V SIM card support.
- 1.8 V as well as 3.0 V memory and I/O support.
- Improved external memory support.
  - SDRAM support.
  - 1.8 V memory support.
- SPI interface.
- Larger keypad, up to 5 x 6.

1.2 Applications

SC6600D provides a single-chip baseband solution to wireless tri-band telephone handsets and data modems conforming to the GSM Release 1999, GSM850, GSM900, DCS1800 and PCS1900.

1.3 General Description

SC6600D is a highly integrated mixed signal baseband processor for GSM/GPRS applications. It consists of an embedded 32-bit microcontroller and an embedded 16-bit DSP core and integrated many GSM/GPRS-specific hardware accelerators and analog functions to simplify the system designs.

The embedded MCU runs a real-time operation system (RTOS), performs the system control functions according to the GSM protocol stack, and services all peripheral components including man-machine interface.

The embedded DSP provides data processing power for many GSM/GPRS-specific physical layer signal processing, including power measurement of the serving and neighboring cells, frequency estimation and timing track, baseband data interleaving/deinterleaving, burst building, channel estimation/equalization, speech encoding/decoding, etc., and controls the operation of ASIC hardware accelerators.

The system timing control provides clocks for the system and controls the mode of the system operations. The system timing control consists of the following parts:

- A master clock input, which is the system clock for normal GSM operations.
- A phase locked loop (PLL), which is used to generate clocks with higher frequencies.
- A real time clock (RTC), which is used to count the seconds, minutes and hours and to maintain the system timing during the power-saving (sleep) mode.
- A system timer, which generates the GSM-specific timing base.
- A system state machine, which controls the system's normal operation and power-saving (sleep) modes.

The baseband RF interface is a complete interface between an RF module and the on-chip digital signal processor (DSP). It consists of the following major parts:

- A transmit path, which converts a bit stream to analog quadrature (I/Q) signals to an RF transceiver.
- A receive path, which converts analog quadrature (I/Q) signals from an RF transceiver to digital signals.
- An event scheduler, which controls the timing of the baseband Tx and Rx actions with the quarter-bit accuracy.

The RF interface is the interface between the baseband chip and an RF module. The RF interface consists of the following parts:

- An RF power amplifier control, which controls the timing of an RF power amplifier ON/OFF as well as its output power.
- An RF serial port, which is used to program control registers inside the RF module.
- RF parallel controls, which form a group of control signals to control the ON/OFF of the RF active components and passive couplers/switches.

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The Viterbi channel equalizer (VE) is a hardware accelerator for recovering the information bits from the baseband digital I/Q data.

The baseband channel encoder/decoder performs encoding and decoding functions for all GSM/GPRS traffic and control channels. It consists of the following major parts:

- A convolution coder (CC), which performs the convolution encoding with 1/2, 1/3 or 1/6 rate.
- A cyclic redundancy coder/decoder (CRC), which generates/checks parity bits for some of the information bits.
- A Viterbi decoder (VA), which performs the decoding for the convolution codes with both hard and soft bits provided from the Viterbi channel equalizer (VE).
- A FIRE decoder, which decodes the FIRE codes for SACCH and some other control channels.

The voice band interface is a complete interface between a microphone/earphone and the DSP, and it consists of the following major parts:

- An uplink path, which converts the analog signal from a microphone to digital signals, performs filtering and outputs the data to the DSP.
- A downlink path, which converts the digital signals from the DSP to analog signals to drive an earphone or a speaker.
- A Digital Audio Interface (DAI), which is primarily used for Full Type Approval (FTA).

The peripheral control section provides Man-Machine-Interface (MMI) for keypad, LCD, etc. and data ports.

The auxiliary Analog-to-Digital Converter (ADC) module provides five input channels that can be used for battery management or other applications.

The auxiliary Digital-to-Analog Converter (DAC) blocks supports Automatic Frequency Control (AFC) and RF power ramping.

The integrated analog baseband processor provides ADCs and DACs for the baseband and voice band up/down links, power management circuits, all auxiliary drivers, PLL, a band-gap reference, LDO regulators and a battery charger.

Proprietary architectures and algorithms were developed for low power ASIC design and power management. Unique techniques are used for noise/offset calibration and cancellation.

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1.4 Block Diagram

Figure 1 shows the chip-level functional block diagram of SC6600D. This chip architecture is based on two processors, an MCU and a DSP, and other functional blocks are connected to one or both of the buses and provide various hardware accelerations and interfaces to other components in the system.

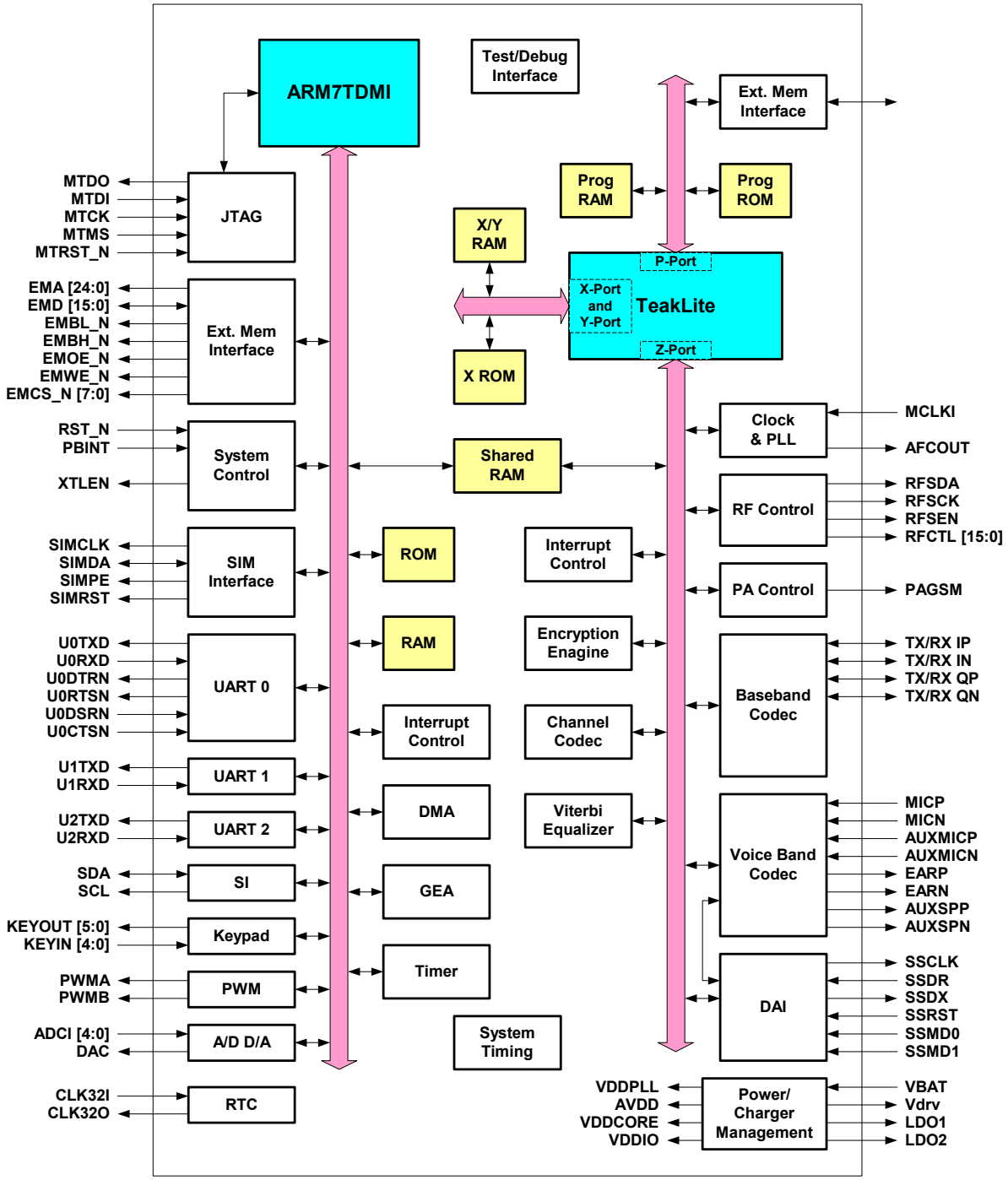

Figure 1: SC6600D chip-level functional block diagram.

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2 Pin Information

This section describes SC6600D external pins. It should be noted that some of the pins have more than one function for different applications. In that case, the function can be selected through control registers.

2.1 Pin Type Description

Table 1 explains the pin type symbols used in the pin lists.

Table 1: I/O pin type description.

Symbol	Type Description
I	Digital input
O	Digital output
O/T	Digital output with tri-state option
VBAT	Power supply input
VDD	VDD for core
VIO	VDDIO, power supply for I/O
VMEM	Power supply for memory I/O
VSIM	Power supply for SIM interface
G	Ground
AI	Analog input
AO	Analog output
AV	Analog VDD
AG	Analog ground

2.2 Pin List by Pin Numbers

Table 2 lists SC6600D pins by pin numbers. This is for the 180-ball package.

Table 2: List of SC6600D pins by pad numbers.

Pad No.	Package Ball No.	Pin Name	Type	Value during Reset	Default Dir	Default Value	Description
1	C2	AUXSPP	AO	O/T	AO	O/T	Auxiliary speaker differential positive output
2	C3	AUXSPN	AO	O/T	AO	O/T	Auxiliary speaker differential negative output (HEAD_P_R)
3	A1	RTCVSS	G	GND	GND	GND	RTC ground
4	B1	CLK32O	AO	-	AO	-	32.768 kHz crystal oscillator output (RTC32KO)
5	C1	CLK32I	AI	-	AI	-	32.768 kHz crystal oscillator input (RTC32KI)
6	D2	RTCVDD	VRTC	VRTC	Power	VRTC	RTC power (1.8 V)
7	E3	AVDD36RF	VBAT	VBAT	Power	VBAT	Power input for LDO1 and LDO2 (3.6 V)
8	D1	VRF	AV	VRF	Power	VRF	RF Power Supply (2.8 V)
9	D3	VLCM	AV	VLCM	Power	VLCM	LCM Power Supply (2.8 V)
10	E2	RST_N	I	Low	AI	VBAT	Asynchronous reset, active low
11	E4	RFSDA	O/T	High	O	High	RF serial bus, data output
12	E1	RFSCK	O/T	High	O	High	RF serial bus, clock output
13	E5	RFSEN	O/T	High	O	High	RF serial bus, enable strobe
14	K5	VSS	G	0	0	0	Core ground
15	K8	VBAT	VBAT	VBAT	VBAT	VBAT	Power input for digital (3.6 V)

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Pad No.	Package Ball No.	Pin Name	Type	Value during Reset	Default Dir	Default Value	Description
16	F3	RFCTL0	O	High	O	High	RF control, RX_PWRON
17	F1	RFCTL1	O	High	O	High	RF control, RX_SYNON
18	F2	RFCTL2	O	Low	O	Low	RF control, RX_RFON
19	G3	RFCTL3	O	High	O	High	RF control, RX_ON
20	G5	RFCTL4	O	Low	O	Low	RF control, RX_CNTL1
21	G4	RFCTL5	O	Low	O	Low	RF control, TX_PWRON
22	G1	RFCTL6	O	Low	O	Low	RF control, TX_ON
23	G2	RFCTL7	O	Low	O	Low	RF control, TX_CNTL1
24	H4	VSSIO	G	0	0	0	IO ground
25	D10	VDDIO	VIO	VIO	VIO	VIO	IO power (3.0 V)
26	H5	RFCTL8	O	Low	O	Low	RF control, TX_CNTL2
27	H1	RFCTL9	O	O/T	O	x	RF control, RX_CNTL2
28	H3	RFCTL10	O	O/T	O	x	RF control, TX_SYNON
29	J1	RFCTL11	O	O/T	O	x	RF control, TX_RFON
30	H2	RFCTL12	O	O/T	O	x	RF control, BAND_SEL [0] or register control
31	J3	EMCS2_N	O	High	O	High	ARM external CS 2
32	J2	EMCS3_N	O	High	O	High	ARM external CS 3
33	J4	XTLEN	O	High	O	High	XTAL enable
34	K4	SYSPD	O	High	O	Low	System power down
35	K1	KEYIN4/A23	O	High	O	Low	ARM external address
36	K3	PBINT	I	High	I	-	Power button interrupt, active high
37	L3	MTDO	O/T	O/T	O	O/T	ARM JTAG data output
38	L1	MTDI	I	-	I	-	ARM JTAG data input
39	K2	MTCK	I	-	I	-	ARM JTAG clodk
40	K5	VSS	G	GND	GND	GND	Core ground
41	M1	MTMS	I	-	I	-	ARM JTAG mode select
42	L2	MTRST_N	I	-	I	-	ARM JTAG reset, active low
43	N1	RFCTL13	O	O/T	O	High	RF control, BAND_SEL [1] or register control
44	K10	VDD	V	VDD	VDD	VDD	Decoupling cap connection pin, core power (1.8 V)
45	F5	VBAT	VBAT	VBAT	VBAT	VBAT	Power input for digital (3.6 V)
46	M3	VSSIO	G	GND	GND	GND	IO ground
47	M2	RFCTL14	O	-	I	-	RF control
48	P1	RFCTL15	O	-	I	-	RF control
49	N3	U0TXD	O	O/T	I	High	ARM UART transmit data output
50	N2	U0RXD	I	-	I	-	ARM UART receive data input
51	P2	GPIO26	I/O	High	I	-	ARM GPIO
52	P3	GPIO27	I/O	High	I	-	ARM GPIO
53	P4	SCL0	I/O	High	O	Low	Serial bus clock
54	N4	GPIO29	I/O	High	O	Low	ARM GPIO29
55	M4	EMA22	I/O	High	O	Low	ARM external address
56	N5	PA4/Boot	O	High	O	High	Severs as NBoot strapping pin function at reset
57	P5	SDA	I/O	O/T	O	Low	Serial bus data
58	M5	U2RXD	I/O	High	I	-	ARM/DSP UART receive data input
59	L5	EMA0	O	O/T	O	0	ARM external address
60	P6	EMA1	O	O/T	O	0	ARM external address
61	L6	EMA2	O	O/T	O	0	ARM external address

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Pad No.	Package Ball No.	Pin Name	Type	Value during Reset	Default Dir	Default Value	Description
62	M6	EMA3	O	O/T	O	0	ARM external address
63	N7	EMA4	O	O/T	O	0	ARM external address
64	N6	EMA5	O	O/T	O	0	ARM external address
65	P7	EMA6	O	O/T	O	0	ARM external address
66	M7	EMA7	O	O/T	O	0	ARM external address
67	G10	VSS	G	GND	GND	GND	Core ground
68	L8	VMEM	VIO	VMEM	VMEM	VMEM	Memory power (3.0 V)
69	N8	EMA8	I/O	O/T	O	0	ARM external address
70	L7	EMA9	I/O	O/T	O	0	ARM external address
71	F5	VBAT	VBAT	VBAT	VBAT	VBAT	Power input for digital (3.6 V)
72	M3	VSSIO	G	GND	GND	GND	IO ground
73	P8	EMA10	O	O/T	O	0	ARM external address
74	M8	EMA11	O	O/T	O	0	ARM external address
75	P9	EMA12	O	O/T	O	0	ARM external address
76	L9	EMA13	O	O/T	O	0	ARM external address
77	M9	EMA14	O	O/T	O	0	ARM external address
78	L10	EMA15	O	O/T	O	0	ARM external address
79	N9	EMA16	O	O/T	O	0	ARM external address
80	P10	EMA17	O	O/T	O	0	ARM external address
81	P11	EMA18	O	O/T	O	0	ARM external address
82	N10	EMA19	O	O/T	O	0	ARM external address
83	K6	VDD	V	VDD	VDD	VDD	Decoupling cap connection pin, core power (1.8 V)
84	M10	EMA20	O	O/T	O	0	ARM external address
85	L11	EMA21	O	O/T	O	0	ARM external address
86	M3	VSSIO	G	GND	GND	GND	IO ground
87	M11	EMBL_N	O	O/T	O	0	ARM byte low select
88	P12	EMBH_N	O	O/T	O	0	ARM byte high select
89	P13	CLKMCU	O	GND	O	Clock	ARM clock
90	K11	VMEM	VIO	VMEM	VMEM	VMEM	Memory power (3.0 V)
91	F4	VSS	G	GND	GND	GND	Core ground
92	N11	EMOE_N	O	High	O	High	ARM external output enable, active low
93	N12	EMWE_N	O	High	O	High	ARM external write enable, active low
94	M13	EMCS_N0	O	High	O	High	ARM external chip select 0, active low
95	M12	EMCS_N1	O	High	O	High	ARM external chip select 1, active low
96	N13	EMD0	I/O	Low	I	-	ARM external data
97	P14	EMD1	I/O	Low	I	-	ARM external data
98	N14	EMD2	I/O	Low	I	-	ARM external data
99	M14	EMD3	I/O	Low	I	-	ARM external data
100	L14	EMD4	I/O	Low	I	-	ARM external data
101	L13	EMD5	I/O	Low	I	-	ARM external data
102	L12	EMD6	I/O	Low	I	-	ARM external data
103	K12	EMD7	I/O	Low	I	-	ARM external data
104	K13	EMD8	I/O	Low	I	-	ARM external data
105	K14	EMD9	I/O	Low	I	-	ARM external data
106	J12	EMD10	I/O	Low	I	-	ARM external data
107	J14	EMD11	I/O	High	I	-	ARM external data
108	J13	EMD12	I/O	High	I	-	ARM external data
109	H12	EMD13	I/O	Low	I	-	ARM external data
110	H14	EMD14	I/O	Low	I	-	ARM external data

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Pad No.	Package Ball No.	Pin Name	Type	Value during Reset	Default Dir	Default Value	Description
111	H11	VBAT	VBAT	VBAT	VBAT	VBAT	Power input for digital (3.6 V)
112	E9	VSSIO	G	GND	GND	GND	IO ground
113	K5	VSS	G	GND	GND	GND	Core ground
114	H13	EMD15	I/O	Low	I	-	ARM external data
115	G12	U1TXD	O	High	O	High	Shared UART output data
116	G14	U1RXD	I	O/T	I	-	Shared UART input data
117	G11	ARMCLK	O	Low	O	Clock	Clock output
118	G13	SIMCLK	O	Low	O	Low	SIM clock output
119	F12	SIMDA	I/O	O/T	I	Low	SIM data
120	F11	VSIM	VSIM	GND	O	GND	SIM power (SIMPE)
121	F10	SIMRST	O	Low	O	Low	SIM reset
122	F14	/CS4	O	High	O	High	ARM external chip select 4, active low
123	F13	KEYOUT0	O	O/T	O	High	Keypad output
124	E10	KEYOUT1	O	O/T	O	High	Keypad output
125	E11	KEYOUT2	O	O/T	O	High	Keypad output
126	E12	KEYOUT3	O	O/T	O	Low	Keypad output
127	E14	KEYOUT4	O	O/T	O	High	Keypad output
128	D12	KEYOUT5	O	O/T	O	High	Keypad output
129	E13	KEYIN0	I	VIO	I	HZ	Keypad input
130	D14	KEYIN1	I	VIO	I	HZ	Keypad input
131	D13	KEYIN2	I	VIO	I	HZ	Keypad input
132	D11	VBAT	VBAT	VBAT	VBAT	VBAT	Power input for digital (3.6 V)
133	C13	KEYIN3	I	VIO	I	HZ	Keypad input
134	C12	VDD	V	VDD	VDD	VDD	Decoupling cap connection pin, core power (1.8 V)
135	D10	VDDIO	VIO	VIO	VIO	VIO	IO power (3.0 V)
136	C11	VSSIO	G	GND	GND	GND	IO ground
137	C11	VSSIO	G	GND	GND	GND	IO ground
138	B12	MCLKI	AI	-	AI	-	Master clock input (13 MHz)
139	C14	AGNDPLL	AG	GND	GND	GND	PLL GND
140	B14	PLLPF	A	-	A	-	PLL low-pass filter
141	B13	AVDDPLL	AV	VPLL	VPLL	VPLL	PLL VDD (1.8 V)
142	B11	TXREF1	A	Low	A	Low	Tx reference voltage
143	A14	TXQP	AI	-	A	-	Tx baseband-Q differential positive output
144	A13	TXQN	AI	-	A	-	Tx baseband-Q differential negative output
145	C10	TXIN	AI	-	A	-	Tx baseband-I differential negative output
146	C9	TXIP	AI	-	A	-	Tx baseband-I differential positive output
147	B10	AVDDBB	AV	AV	AV	AV	Decoupling cap connection pin, baseband VDD
148	A12	AGNDBB	AG	GND	GND	GND	Baseband GND
149	A11	RXREF1	A	-	A	-	Rx reference voltage
150	D9	AVDD36	AV	VBAT	VBAT	VBAT	AVDD 3.6 V LDO input
151	E8	VDRV	AO	-	AO	-	Battery charger control
152	A10	ISENSE	AI	-	AI	-	Battery charger current sense input
153	A9	VCHG	AV	GND	GND	GND	Battery charger power supply (5.0 V)
154	B9	PROG	AIO	GND	A	GND	Battery charger current programming

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Pad No.	Package Ball No.	Pin Name	Type	Value during Reset	Default Dir	Default Value	Description
155	A8	AUXREF	A	Low	A	-	Reference voltage filter
156	B8	AGNDAUX	AG	GND	GND	GND	Auxiliary GND
157	D8	AFCOUT	AO	A/T	AO	A/T	Automatic frequency control output
158	C8	PAGSM	AO	A/T	AO	A/T	Power ramping control for GSM
159	E7	AVDDAUX	AV	AV	AV	AV	Decoupling cap connection pin, auxiliary VDD
160	C7	ADCI4	AI	-	AI	-	Auxiliary ADC input 4
161	A7	ADCI3	AI	-	AI	-	Auxiliary ADC input 3
162	B7	ADCI2	AI	-	AI	-	Auxiliary ADC input 2
163	C6	ADCI1	AI	-	AI	-	Auxiliary ADC input 1
164	E6	ADCI0	AI	-	AI	-	Auxiliary ADC input 0
165	D9	AVDD36	AV	VBAT	VBAT	VBAT	AVDD 3.6 V LDO input
166	D6	VR_BG	A	-	A	-	Band gap reference voltage
167	A6	DGND3V	G	GND	GND	GND	Digital ground
168	B6	DVDD3V	V	AV	AV	AV	Decoupling cap connection pin, digital power (2.8 V)
169	D4	MICBIAS	AO	Low	A	Low	MIC bias output
170	D5	VBREF1	A	Low	A	Low	Voice band reference voltage
171	B5	AUXMICP	AI	-	AI	-	Auxiliary microphone differential positive input
172	A5	MICP	AI	-	AI	-	Microphone differential positive input
173	A4	MICN	AI	-	AI	-	Microphone differential negative input
174	C5	AUXMICN	AI	-	AI	-	Auxiliary microphone differential negative input
175	A3	AVDDVB	AV	AV	AV	AV	Decoupling cap connection pin, voice band VDD
176	C4	AGNDVB	AG	GND	GND	GND	Voice band GND
177	B4	EARN	AO	A/T	AO	A/T	Earphone differential negative output (HEAD_P_L)
178	B3	EARP	AO	A/T	AO	A/T	Earphone differential positive output
179	B2	AGNDVBO	AG	GND	GND	GND	Voice band GND
180	A2	AVDDVBO	AV	AV	AV	AV	Decoupling cap connection pin, analog power (2.8 V) for voice band output drivers

2.3 Pin List by Functions

Table 3 lists the pins by their functions.

Table 3: List of SC6600 pins by functions.

Bonding Pad No.	Package Ball No.	Pin Name	Type	Description
Voice band interface (14 pins)				
172	A5	MICP	AI	Microphone differential positive input
173	A4	MICN	AI	Microphone differential negative input
177	B4	EARN	AO	Earphone differential negative output
178	B3	EARP	AO	Earphone differential positive output
171	B5	AUXMICP	AI	Auxiliary microphone differential positive input

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Bonding Pad No.	Package Ball No.	Pin Name	Type	Description
174	C5	AUXMICN	AI	Auxiliary microphone differential negative input
1	C2	AUXSPP	AO	Auxiliary speaker differential positive output
2	C3	AUXSPN	AO	Auxiliary speaker differential negative output
170	D5	VBREF1	A	Voice band reference voltage
175	A3	AVDDVB	AV	Voice band power (2.8 V), decoupling cap only
176	B4	AGNDVB	AG	Voice band ground
180	A2	AVDDVBO	AV	Analog power (2.8 V) for voice band output drivers, decoupling cap only
179	B2	AGNDVBO	AG	Voice band ground
169	D4	MICBIAS	AO	MIC bias output
RTC (4 pins)				
3	A1	RTCVSS	G	RTC ground
4	B1	CLK32O	O	32.768 kHz crystal oscillator output
5	C1	CLK32I	I	32.768 kHz crystal oscillator input
6	D2	RTCVDD	V	RTC power (1.8 V)
System control (4 pins)				
10	E2	RST_N	I	Asynchronous reset, active low
33	J4	XTLEN	O	XTAL enable
34	K4	SYSPD	O	System power down
36	K3	PBINT	I	Power button interrupt, active high
RF serial port (3 pins)				
11	E4	RFSDA	O/T	RF serial bus, data output
12	E1	RFSCK	O/T	RF serial bus, clock output
13	E5	RFSEN	O/T	RF serial bus, enable strobe
RF control (16 pins)				
16	F3	RFCTL0	O	RF control, RX_PWRON (shared with EMCS_N5)
17	F1	RFCTL1	O	RF control, RX_SYNON (shared with EMCS_N6)
18	F2	RFCTL2	O	RF control, RX_RFON
19	G3	RFCTL3	O	RF control, RX_ON (shared with EMCS_N7)
20	G5	RFCTL4	O	RF control, RX_CNTL1
21	G4	RFCTL5	O	RF control, TX_PWRON
22	G1	RFCTL6	O	RF control, TX_ON
23	G2	RFCTL7	O	RF control, TX_CNTL1
26	H5	RFCTL8	O	RF control, TX_CNTL2
27	H1	RFCTL9	O	RF control, RX_CNTL2
28	H3	RFCTL10	O	RF control, TX_SYNON
29	J1	RFCTL11	O	RF control, TX_RFON
30	H2	RFCTL12	O	RF control, BAND_SEL [0] or register control
43	N1	RFCTL13	O	RF control, BAND_SEL [1] or register control
47	M2	RFCTL14	O	RF control, TX_CNTL1 (shared with GPIO22)
48	P1	RFCTL15	O	RF control, TX_SYNON (shared with GPIO23)
UART 0 (6 pins)				
49	N3	U0TXD	O	ARM UART transmit data output
50	N2	U0RXD	I	ARM UART receive data input
37	L3	U0DTRN	O	ARM UART hardware flow control
38	L1	U0RTSN	O	ARM UART hardware flow control
39	K2	U0DSRN	I	ARM UART hardware flow control
41	M1	U0CTSN	I	ARM UART hardware flow control
UART 2 (6 pins)				
56	N5	U2TXD	O	ARM/DSP UART transmit data output
58	M5	U2RXD	I	ARM/DSP UART receive data input
27	H1	U2DTRN	O	ARM/DSP UART hardware flow control
28	H3	U2RTSN	O	ARM/DSP UART hardware flow control
29	J1	U2DSRN	I	ARM/DSP UART hardware flow control

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Bonding Pad No.	Package Ball No.	Pin Name	Type	Description
30	H2	U2CTSN	I	ARM/DSP UART hardware flow control
PWM (3 pin)				
54	N4	PWMA	O	ARM PWM output A
53	P4	PWMB	O	ARM PWM output B (shared with SCL)
42	L2	PWMB	O	ARM PWM output B (shared with MTRST_N)
JTAG (5 pins, shared with UART 0 and PWMB)				
37	L3	MTDO	O/T	ARM JTAG data output
38	L1	MTDI	I	ARM JTAG data input
39	K2	MTCK	I	ARM JTAG clock
41	M1	MTMS	I	ARM JTAG mode select
42	L2	MTRST_N	I	ARM JTAG reset, active low
GPIO (5 pins)				
51	P2	GPIO26	I/O	ARM GPIO
52	P3	GPIO27	I/O	ARM GPIO
54	N4	GPIO29	I/O	ARM GPIO
122	F14	GPIO46	I/O	ARM GPIO (shared with EMCS_N4)
Two-wire serial port (2 pins)				
57	P5	SDA	I/O	Serial bus data (shared with EMA24)
58	M5	SCL	I/O	Serial bus clock
ARM external memory interface (50 pins)				
59	L5	EMA0	O	ARM external address
60	P6	EMA1	O	ARM external address
61	L6	EMA2	O	ARM external address
62	M6	EMA3	O	ARM external address
63	N7	EMA4	O	ARM external address
64	N6	EMA5	O	ARM external address
65	P7	EMA6	O	ARM external address
66	M7	EMA7	O	ARM external address
69	N8	EMA8	O	ARM external address
70	L7	EMA9	O	ARM external address
73	P8	EMA10	O	ARM external address
74	M8	EMA11	O	ARM external address
75	P9	EMA12	O	ARM external address
76	L9	EMA13	O	ARM external address
77	M9	EMA14	O	ARM external address
78	L10	EMA15	O	ARM external address
79	N9	EMA16	O	ARM external address
80	P10	EMA17	O	ARM external address
81	P11	EMA18	O	ARM external address
82	N10	EMA19	O	ARM external address
84	M10	EMA20	O	ARM external address
85	L11	EMA21	O	ARM external address
55	M4	EMA22	O	ARM external address
35	K1	KEYIN4/A23	O	ARM external address (shared with KEYIN4)
57	P5	EMA24	O	ARM external address (shared with SDA)
56	N5	PA4/NBoot	O	Severs as NBoot strapping pin function at reset
87	M11	EMBL_N	O	ARM byte low select
88	P12	EMBH_N	O	ARM byte high select
89	P13	CLKMCU	O	ARM clock
117	G11	ARMCLK	O	ARM clock
92	N11	EMOE_N	O	ARM external output enable, active low
93	N12	EMWE_N	O	ARM external write enable, active low
94	M13	EMCS_N0	O	ARM external chip select 0, active low
95	M12	EMCS_N1	O	ARM external chip select 1, active low

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Bonding Pad No.	Package Ball No.	Pin Name	Type	Description
31	J3	EMCS_N2	O	ARM external chip select 2, active low
32	J2	EMCS_N3	O	ARM external chip select 3, active low
122	F14	EMCS_N4	O	ARM external chip select 4, active low (also GPIO46)
16	F3	EMCS_N5	O	ARM external chip select 5, active low (also RFCTL0)
17	F1	EMCS_N6	O	ARM external chip select 6, active low (also RFCTL1)
19	G3	EMCS_N7	O	ARM external chip select 7, active low (also RFCTL3)
96	N13	EMD0	I/O	ARM external data
97	P14	EMD1	I/O	ARM external data
98	N14	EMD2	I/O	ARM external data
99	M14	EMD3	I/O	ARM external data
100	L14	EMD4	I/O	ARM external data
101	L13	EMD5	I/O	ARM external data
102	L12	EMD6	I/O	ARM external data
103	K12	EMD7	I/O	ARM external data
104	K13	EMD8	I/O	ARM external data
105	K14	EMD9	I/O	ARM external data
106	J12	EMD10	I/O	ARM external data
107	J14	EMD11	I/O	ARM external data
108	J13	EMD12	I/O	ARM external data
109	H12	EMD13	I/O	ARM external data
110	H14	EMD14	I/O	ARM external data
114	H13	EMD15	I/O	ARM external data
UART 1 (2 pins)				
115	G12	U1TXD	O	Shared UART output data
116	G14	U1RXD	I	Shared UART input data
SIM interface (4 pins)				
118	G13	SIMCLK	O	SIM clock output
119	F12	SIMDA	I/O	SIM data
120	F11	VSIM	VSIM	SIM power
121	F10	SIMRST_N	O	SIM reset
Keypad interface (11 pins)				
123	F13	KEYOUT0	O	Keypad output
124	E10	KEYOUT1	O	Keypad output
125	E11	KEYOUT2	O	Keypad output
126	E12	KEYOUT3	O	Keypad output
127	E14	KEYOUT4	O	Keypad output
128	D12	KEYOUT5	O	Keypad output
129	E13	KEYIN0	I	Keypad input
130	D14	KEYIN1	I	Keypad input
131	D13	KEYIN2	I	Keypad input
133	C13	KEYIN3	I	Keypad input
35	K1	KEYIN4	I	Keypad input (shared with EMA23)
Master clock interface (2 pins)				
138	B12	MCLKI	AI	Master clock input (13 MHz)
157	D8	AFCOUT	AO	Automatic frequency control output
PLL (3 pins)				
139	C14	AGNDPLL	AG	PLL ground
140	B14	PLLPF	A	PLL low-pass filter
141	B13	AVDDPLL	AV	PLL power (1.8 V)
Baseband analog interface (8 pins)				
142	B11	TXREF1	A	Tx reference voltage
143	A14	TXQP	AI	Tx/Rx baseband-Q differential positive output/input
144	A13	TXQN	AI	Tx/Rx baseband-QN differential negative output/input
145	C10	TXIN	AI	Tx/Rx baseband-IN differential negative output/input

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Bonding Pad No.	Package Ball No.	Pin Name	Type	Description
146	C9	TXIP	AI	Tx/Rx baseband-I differential positive output/input
147	B10	AVDDBB	AV	Baseband power (2.8 V), decoupling cap only
148	A12	AGNDBB	AG	Baseband ground
149	A11	RXREF1	A	Rx reference voltage
PA control (1 pin)				
158	C8	PAGSM	AO	Power ramping control for GSM
Auxiliary ADC (8 pins)				
160	C7	ADCI4	AI	Auxiliary ADC input 4
161	A7	ADCI3	AI	Auxiliary ADC input 3
162	B7	ADCI2	AI	Auxiliary ADC input 2
163	C6	ADCI1	AI	Auxiliary ADC input 1
164	E6	ADCI0	AI	Auxiliary ADC input 0
159	E7	AVDDAUX	AV	Auxiliary power (2.8 V), decoupling cap only
156	B8	AGNDAUX	AG	Auxiliary ground
155	A8	AUXREF	A	Auxiliary reference voltage filter
Charger (4 pins)				
151	E8	VDRV	AO	Battery charger control
152	A10	ISENSE	AI	Battery charger current sense input
153	A9	VCHG	AV	Battery charger power supply (5.0 V)
154	B9	PROG	AIO	Battery charger current programming
LDO (3 pins)				
9	D3	VLCM	AO	LCM Power Supply (2.8 V)
8	D1	VRF	AO	RF Power Supply (2.8 V)
7	E3	AVDD36RF	AV	VBAT 3.6 V LDO input for analog
Misc. analog (2 pin)				
166	D6	VR_BG	A	Band gap reference voltage, decoupling cap only
168	B6	DVDD3V	V	Digital VDD (2.8 V)
167	A6	DGND3V	G	Digital ground
Core power supply, cap only (3 pins)				
44	K6	VDD	V	Digital core power supply (1.8 V), decoupling cap only
83	K10	VDD	V	Digital core power supply (1.8 V), decoupling cap only
134	C12	VDD	V	Digital core power supply (1.8 V), decoupling cap only
I/O power supply, 3 V (2 pins)				
25	D10	VDDIO	V	Digital I/O power supply (3.0 V)
135	J5	VDDIO	V	Digital I/O power supply (3.0 V)
Memory power supply, 3 V (2 pins)				
68	L8	VMEM	V	Memory power supply (3.0 V)
90	K11	VMEM	V	Memory power supply (3.0 V)
Battery power supply, 3.6 V (8 pins)				
15	D11	VBAT	V	Power supply input for digital (3.6 V)
45	F5	VBAT	V	Power supply input for digital (3.6 V)
71	H11	VBAT	V	Power supply input for digital (3.6 V)
111	K8	VBAT	V	Power supply input for digital (3.6 V)
132	L4	VBAT	V	Power supply input for digital (3.6 V)
150	D7	AVDD36	V	Power supply input for analog (3.6 V)
165	D9	AVDD36	V	Power supply input for analog (3.6 V)
7	E3	AVDD36RF	V	Power supply input for output LDO (3.6 V)
Ground (13 pins)				
14	J10	VSS	G	Digital core ground
40	K7	VSS	G	Digital core ground
67	G10	VSS	G	Digital core ground
91	F4	VSS	G	Digital core ground
113	K5	VSS	G	Digital core ground
24	E9	VSSIO	G	Digital I/O ground

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Bonding Pad No.	Package Ball No.	Pin Name	Type	Description
46	H4	VSSIO	G	Digital I/O ground
72	H10	VSSIO	G	Digital I/O ground
86	J11	VSSIO	G	Digital I/O ground
112	K9	VSSIO	G	Digital I/O ground
136	M3	VSSIO	G	Digital I/O ground
137	C11	VSSIO	G	Digital I/O ground

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2.4 Package Pin Map

Figure 2 shows the pin configuration of the bonding pad number and the package ball number on the 180-ball package.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14
A	*RTCVSS*	**AVDDVBO**	**AVDDVB**	MICN	MICP	*DGND3V*	ADCI3	AUXREF	**VCHG**	ISENSE	RXREF1	*AGNDBB (PSUB)*	TXQN	TXQP
B	CLK32O	*AGNDVBO*	EARP	EARN	AUXMICP	**DVDD3V**	ADCI2	*AGNDAUX*	PROG	**AVDDBB (NWELL)**	TXREF1	MCLKI	**AVDDPLL**	PLLPF
C	CLK32I	AUXSPP	AUXSPN	*AGNDVB*	AUXMICN	ADCI1	ADCI4	PAGSM	TXIP	TXIN	*VSSIO*	**VDD**	KEYIN3	*AGNDPLL*
D	**LDO1**	**RTCVDD**	**LDO2**	MICBIAS	VBREF1	VR_BG	**AVDD36**	AFCOUT	**AVDD36**	**VDDIO**	**VBAT**	KEYOUT5	KEYIN2	KEYIN1
E	RFSCK	RST_N	**AVDD36RF**	RFSDA	RFSEN	ADCI0	**AVDDAUX**	VDRV	*VSSIO*	KEYOUT1	KEYOUT2	KEYOUT3	KEYIN0	KEYOUT4
F	RFCTL1	RFCTL2	RFCTL0	*VSS*	**VBAT**					SIMRST	**VSIM**	SIMDA	KEYOUT0	GPIO46
G	RFCTL6	RFCTL7	RFCTL3	RFCTL5	RFCTL4					*VSS*	ARMCLK	U1TXD	SIMCLK	U1RXD
H	RFCTL9	RFCTL12	RFCTL10	*VSSIO*	RFCTL8					*VSSIO*	**VBAT**	EMD13	EMD15	EMD14
J	RFCTL11	EMCS3_N	EMCS2_N	XTLEN	**VDDIO**					*VSS*	VSSIO	EMD10	EMD12	EMD11
K	EMA23	U0DSRN	PBINT	SYSPD	*VSS*	**VDD**	*VSS*	**VBAT**	*VSSIO*	**VDD**	**VMEM**	EMD7	EMD8	EMD9
L	U0RTSN	PWMB	U0DTRN	**VBAT**	EMA0	EMA2	EMA9	**VMEM**	EMA13	EMA15	EMA21	EMD6	EMD5	EMD4
M	U0CTSN	RFCTL14	*VSSIO*	EMA22	SCL	EMA3	EMA7	EMA11	EMA14	EMA20	EMBL_N	EMCS1_N	EMCS0_N	EMD3
N	RFCTL13	U0RXD	U0TXD	GPIO29	PWMA	EMA5	EMA4	EMA8	EMA16	EMA19	EMOE_N	EMWE_N	EMD0	EMD2
P	RFCTL15	GPIO26	GPIO27	GPIO28	SDA	EMA1	EMA6	EMA10	EMA12	EMA17	EMA18	EMBH_N	CLKMCU	EMD1

BOLD Ext. Power **BOLD** Ext. Power **BOLD** Ext. Power **BOLD** Power *ITALIC* Ground Leve

Figure 2: Pin configuration.

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3 Electrical Specifications

3.1 DC Specifications

3.1.1 Absolute Maximum Ratings

The functionality of SC6600D is subject to the absolute maximum/minimum values listed in Table 4.

Table 4: Absolute maximum ratings of SC6600D.

Symbol	Parameter	Min.	Max.	Unit
AVDD36	Supply voltage from a battery	3.3	4.2	V
V_{DI}	Input voltage on any digital input	-0.5	3.6	V
V_{AI}	Input voltage on any analog input	-0.5	3.3	V
I_{AI2}	DC drive current for EARP, EARN, AUXSPP and AUXSPN		60	mA
P_{total}	Total power consumption	–	200	mW
T_a	Ambient temperature	-45	+95	°C
$T_{storage}$	Storage temperature	-65	+125	°C

3.1.2 Recommended Operating Conditions

SC6600D is recommended to operate under the conditions list in Table 5.

Table 5: Recommended operating conditions.

Symbol	Parameter	Min.	Max.	Unit
VBAT	Supply voltage from a battery	3.3	4.2	V
AVDD36	Supply voltage from a battery, for analog	3.3	4.2	V
AVDD36RF	Supply voltage from a battery, for RF LDO	3.3	4.2	V
RTCVDD	Supply voltage for RTC	1.6	2.0	V
$T_{ambient}$	Ambient operating temperature	-30	+70	°C

3.1.3 Thermal Characteristics

The thermal characteristics are as shown in Table 6.

Table 6: Thermal characteristics.

Symbol	Parameter	Condition	Value	Unit
Theta JA	Junction-to-Ambient thermal resistance	Air flow: 0 m/sec	40	DegC/watt

3.1.4 DC Characteristics

SC6600D is fabricated with a 0.18 μm CMOS technology. The typical core voltage (VDD) is 1.8 V and the I/O supply (VDDIO) is typically at 3 V. The analog circuits are typically powered at 2.8 V. The core and analog power supplies are provided by the on-chip LDOs. The external battery can be connected directly to pin AVDD36, AVDD36RF and VBAT. The VDD pins can be left open or connected with a decoupling capacitor to ground (VSS, VSSIO).

For the following table, T_{amb} = -40 to +85 °C, VSS = 0 V (ground), AVDD36 = 3.6 V, and all voltages are measured with respect to VSS, unless otherwise specified.

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Table 7: DC characteristics.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Total supply voltage: pins VBAT						
VBAT	Total supply voltage		3.3	3.6	4.2	V
$I_{standby\ (tot)}$	Total standby current	VBAT is connected with AVDD36 and AVDD36RF.	–	1.0	–	mA
P_{avg}	Average active power consumption	VBAT is connected with AVDD36 and AVDD36RF. VDD = 1.8 V AVDD = 2.8 V	–	100	–	mW
Digital supply voltage: internal VDDIO						
VDDIO	Digital I/O supply voltage		2.7	3.0	3.3	V
Digital supply voltage: internal VMEM						
VMEM	Memory interface supply voltage		2.7	3.0	3.3	V
Digital supply voltage: internal VDD						
VDD	Digital core supply voltage		1.6	1.8	2.0	V
Digital input						
V_{IL}	Input voltage LOW-level		0	–	0.3VDDIO	V
V_{IH}	Input voltage HIGH-level		0.7VDDIO	–	VDDIO	V
I_{LI}	Input leakage current		–	±2	–	µA
Digital output						
V_{OL}	Output voltage LOW-level	At I_{sink} = 2,4,6,10 mA (prog)	–	–	0.3VDDIO	V
V_{OH}	Output voltage HIGH-level	At I_{source} = 2,4,6,10 mA (prog)	0.7VDDIO	–	–	V
Analog supply voltage: pins AVDD36						
AVDD36	Analog supply voltage		3.3	3.6	4.2	V
I_{AVDD36}	Analog supply current	AVDD = 2.8 V All analog blocks are active, but no load at EARP, EARN, AUXSPP and AUXSPN	–	5	–	mA
Analog supply voltage: internal AVDD						
AVDD	Analog core supply voltage		2.5	2.8	3.1	V
RTC supply: pin RTCVDD						
RTCVDD	Supply voltage			1.8		V
I_{RTCVDD}	Supply current			20		µA

3.2 AC Specifications

For the following tables, T_{amb} = -40 to +85 °C, VSS = 0 V (ground), AVDD36 = 3.6 V, and all voltages are measured with respect to VSS, unless otherwise specified.

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Table 8: AC characteristics.

Symbol	Parameter	Conditions	Min.	Typical	Max.	Unit
f_{mclk}	Master clock frequency		–	13	–	MHz
f_{rtcclk}	Real-time clock frequency		–	32.768	–	kHz
Digital input						
C_I	Input capacitance		–	3	–	pF
Digital output						
T_R	Output rise time	Output load = 20 pF	2	–	5	ns
T_F	Output fall time	Output load = 20 pF	2	–	5	ns
Master clock input						
V_{mclk}	Master clock amplitude	AC coupling		–	0.9	V
δ_{mclk}	Master clock duty cycle		40	–	60	%

3.2.1 Master Clock MCLKI Timing

The master clock is input from pin MCLKI.

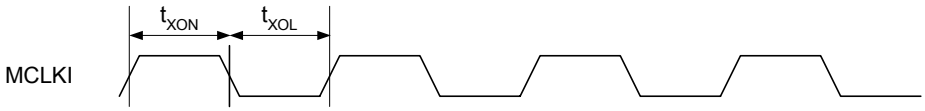

Figure 3: MCLKI Timing Parameters.

Table 9: MCLKI Timing Parameters.

Symbol	Parameter	Min	Typical	Max	Unit
t_{XOH}	MCLKI logic high	–	38.46	–	ns
t_{XOL}	MCLKI logic low	–	38.46	–	ns

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3.2.2 Three-Wire Serial Interface Timing

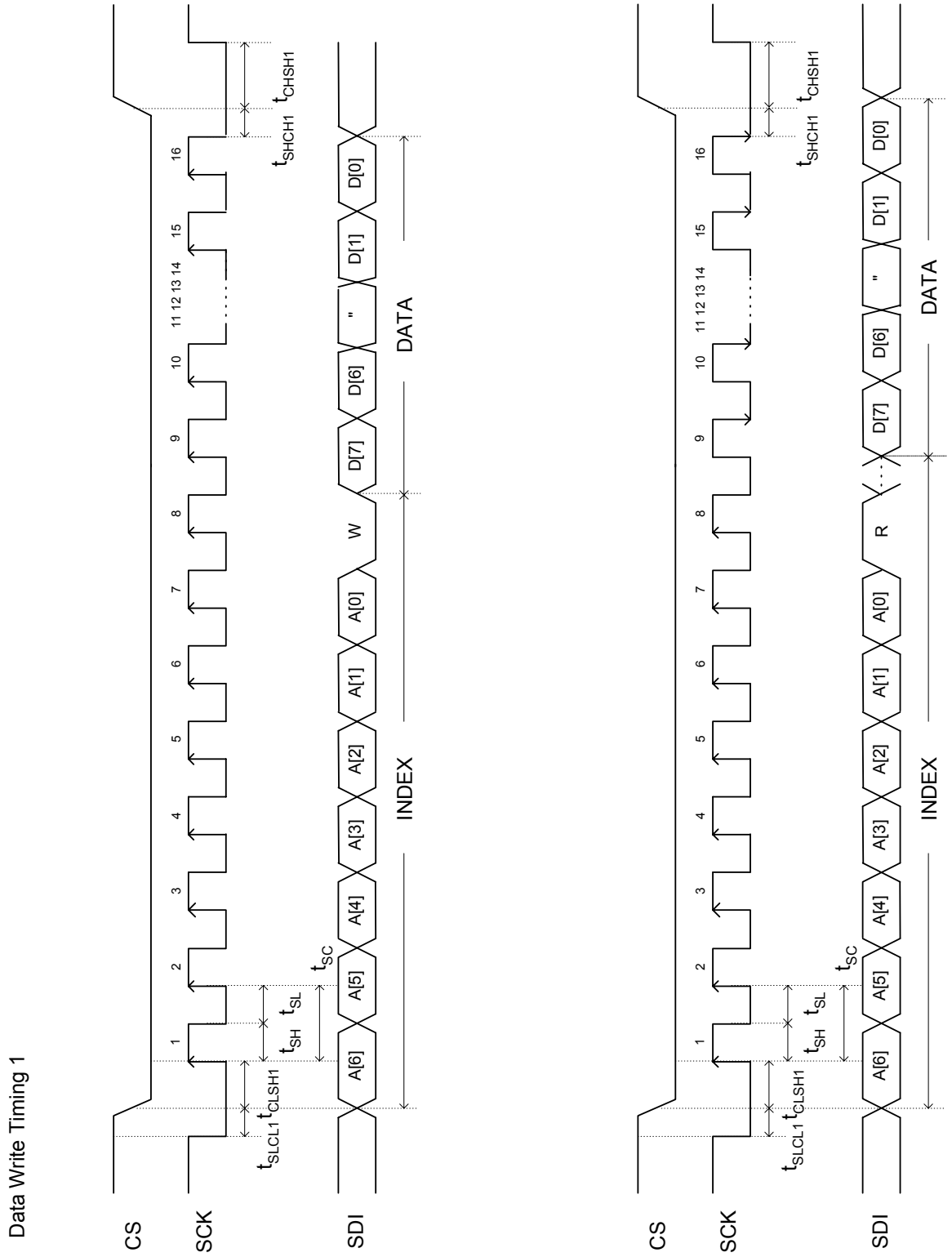

Figure 4: Three-wire serial interface timing parameters (mode 1).

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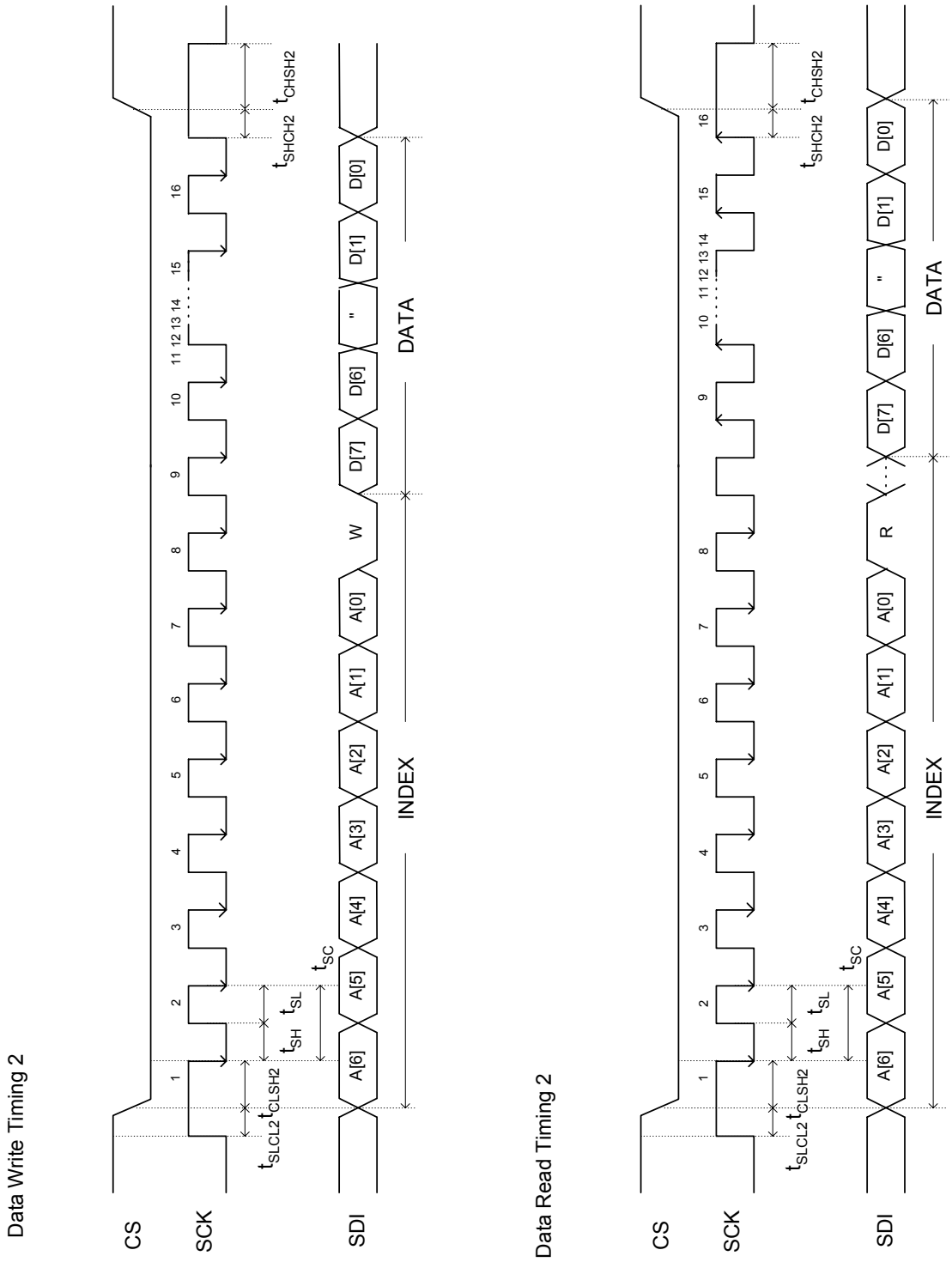

Figure 5: Three-wire serial interface timing parameters (mode 2).

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Table 10: Three-wire serial interface timing parameters.

Symbol	Parameter	Min	Max	Unit
t_{CLSL1}	Chip select low to SCK low	T	–	ns
t_{CLSH1}	Chip select low to SCK high	T	–	ns
t_{CLSL2}	Chip select low to SCK low	T	–	ns
t_{CLSH2}	Chip select low to SCK high	T	–	ns
t_{SH}	SCK high pulse width	N*T/2	–	ns
t_{SL}	SCK low pulse width	N*T/2	–	ns
t_{SC}	SCK cycle time	N*T	–	ns
t_{SHCH1}	SCK high to chip select high	T	–	ns
t_{CHSH1}	Chip select high to SCK high	T	–	ns
t_{SHCH2}	SCK high to chip select high	T	–	ns
t_{CHSH2}	Chip select high to SCK high	T	–	ns

Note:

T: the MCU clock cycle time
N: register programmable

3.2.3 JTAG Timing

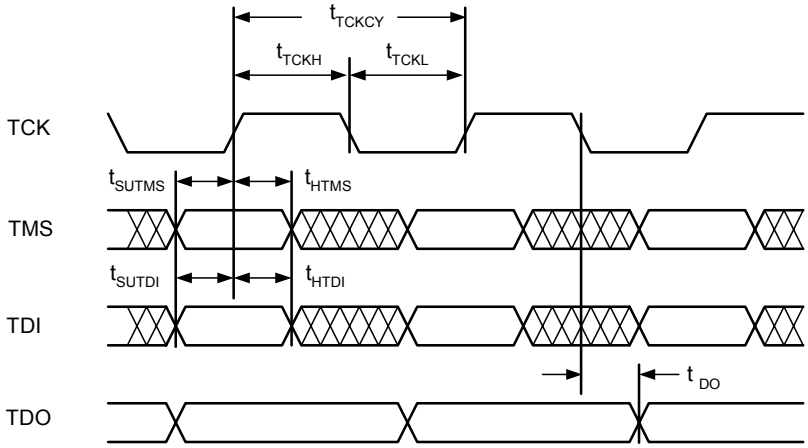

Figure 6: JTAG Interface Timing

Table 11: JTAG Interface Timing

Symbol	Parameter	Min	Typical	Max	Units
t_{TCKCY}	TCK period	?	–	–	ns
t_{TCKH}	TCK pulse width high	?	–	–	ns
t_{TCKL}	TCK pulse width low	?	–	–	ns
t_{SUTMS}	TMS Input Set-up Time	?	–	–	ns
t_{HTMS}	TMS Input Hold Time	?	–	–	ns
t_{SUTDI}	TDI Input Set-up Time	?	–	–	ns
t_{HTDI}	TDI Input Hold Time	?	–	–	ns
t_{DO}	TDO Data Output Delay	–	–	?	ns

3.3 Performance Specifications

This section specifies the performance of some major SC6600D modules.

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3.3.1 Baseband

3.3.1.1 Baseband Transmit Path

The outputs of GMSK modulator are converted to analog levels by 10-bit D/A Converters (DAC), and then passed to an analog Butterworth low pass filter. Each analog part has special offset cancellation.

Table 12: Performance of the baseband transmit path.

Parameter	Conditions/Comments	Min.	Typical	Max.	Unit
Transmission buffer length			160		bits
GMSK modulator					
Input data word rate			270.833		kHz
I/Q interpolation output size			10		bits
DAC					
Number of Channels			2		
Resolution			10		bits
GMSK phase trajectory error					
RMS error	Including analog filter			1.5	°
Peak error				7	°
LP analog filter					
Cutoff frequency (3 dB)			150 ± 25%		kHz
Group delay				9	μsec
I/Q mismatch					
I/Q amplitude mismatch				0.2	dB
I/Q phase mismatch				0.1	°
Maximum differential output voltage	TX_B [1:0] = 00		±0.6		V
	TX_B [1:0] = 10		±0.9		
	TX_B [1:0] = 01		±1.2		
	TX_B [1:0] = 11		±1.5		
Output common mode voltage			1.3		V
DC offset				10	mV
Minimum load resistance					
Single-ended		100			kΩ
Differential		50			kΩ
Maximum load Capacitance					
Single-ended				50	pF
Differential				50	pF
Relative output power	Complies with GSM spectral mask				
	0 – 100 kHz	-3		0	dB
	200 kHz			-32	
	250 kHz			-35	
	400 kHz			-63	
	600 kHz			-71	
	1200 kHz			-71	
	> 1800 kHz			-71	

3.3.1.2 Baseband Receive Path

The differential I/Q signal from the RF module is first amplified by a programmable gain amplifier (PGA). After the amplification, the signal is modulated to single-bit words by Σ-Δ modulator at a frequency much higher than the Nyquist rate. Then the signal passes through a digital filter. Each analog part has special offset cancellation.

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Table 13: Performance of the baseband receive path.

Parameter	Conditions/Comments	Min.	Typical	Max.	Unit
PGA					
Input common mode signal range		0.6		1.8	V
Input gain control range	2 dB steps controlled by 4 digital bits	0		18	dB
Gain resolution			2		dB
Gain control linearity				±1	dB
Maximum analog input range after PGA	Differential			±1.8	V
Input sampling frequency			6.5		MHz
Analog input anti-aliasing LPF					
3-dB single sided bandwidth			500		kHz
Output data					
Word rate			270.833		kHz
Dynamic range		66			dB
Signal to (noise + distortion) ratio			60		dB
Gain mismatch between I/Q channels				±0.15	dB
Absolute group delay			20		µs
Group delay between I/Q channels (0 kHz – 100 kHz)				5	ns

3.3.2 Voice Band

3.3.2.1 Voice Band Uplink ADC

The performance of the voice band uplink ADC is as shown in Table 14.

Table 14: Performance of the voice band ADC.

Parameter	Conditions/Comments	Min.	Typ.	Max.	Units
Input common mode range		0.6		1.8	V
PGA gain range		9		42	dB
PGA gain step size			3		dB
Maximum analog input range after PGA	Differential			±1.5	V
Digital audio output sample rate			8		kHz
ADC resolution		13			bits
ADC signal to (noise + distortion) ratio			62		dB
Digital output word			16		bits

3.3.2.2 Voice Band Downlink DAC

The performance of the voice band downlink DAC is as shown in Table 15.

Table 15: Performance of the voice band DAC.

Parameter	Conditions/Comments	Min.	Typ.	Max.	Units
Digital audio input sample rate			8		kHz
Input digital word			16		bits
DAC resolution			13		bits
DAC signal to noise plus distortion ratio			62		dB
Analog audio output					
Low stop band rejection (< 100		20			dB

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Parameter	Conditions/Comments	Min.	Typ.	Max.	Units
Hz)					
Low passband edge (0.5 dB down from passband level)		120		150	Hz
High pass band edge (0.5 dB down from passband level)		3.4		3.7	kHz
High stop band rejection (> 4500 Hz)		35			dB
Volume Control (for each of normal and auxiliary output)					
Gain range		-21		12	dB
Gain step size			3		dB
Minimum load resistance					
Single ended		16			Ω
Differential		16			Ω
Output amplifier					
Maximum differential output voltage			±1.4		V
Maximum single-ended output voltage			1.4		V
Output common mode voltage			1.1		V
Earpiece mute switch attenuation		-40			dB

3.3.3 Phase-Locked Loop (PLL)

The phase-locked loop (PLL) is used for frequency synthesizers to generate different clocks. The VCO clock is divided by a programmable ”M”, and the divided clock is phase-locked to an external reference clock divided by a programmable “N”. The result is the output clock of the PLL at a frequency M/N times the reference clock frequency. The values for M and N can each range from 2 to 256.

fout = fin * PLLMN[15:8] / PLLMN[7:0]

Table 16: Performance of the phase-locked loop (PLL only).

Parameter	Conditions/Comments	Min.	Typ.	Max.	Unit
Input reference			13/26		MHz
Frequency Range		30		130	MHz
Long term jitter	All other circuits on			1	ns/s
Short term jitter	All other circuits on			150	ps/cycle
Settling time	External filter capacitor 500 pF		100	200	µs
Sleep mode	Yes				

3.3.4 Auxiliary Digital-to-Analog Converters

3.3.4.1 Automatic Frequency Control (AFC)

Parts of the AFC are a 10-bit D/A converter and a programmable gain output driver. Special offset cancellation is applied in the AFC DAC.

Table 17: Performance of the AFC DAC.

Parameter	Conditions/Comments	Min.	Typ.	Max.	Unit
Resolution			10		bits
Integral non-linearity			±3		LSB
Differential non-linearity			±2		LSB
Settling time			4		µs

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Parameter	Conditions/Comments	Min.	Typ.	Max.	Unit
Gain range		1.5		2	x
Minimum output voltage	Gain = 2		0.2		V
Maximum output voltage	Gain = 2		2.6		V
Minimum load resistance			50		kΩ
Maximum load capacitance			50		pF

3.3.4.2 RF Power Ramping Control DAC

The RF power amplifier control (APC) consists of a 10-bit D/A converter and a programmable-gain output driver. Special offset cancellation is applied in the DAC.

Table 18: Performance of the RF power ramping control DAC.

Parameter	Conditions/Comments	Min.	Typ.	Max.	Units
Resolution			10		bits
Integral non-linearity			±3		LSB
Differential non-linearity			±2		LSB
Settling time			4		μs
Gain range		1.5		2	x
Minimum output voltage	Gain = 1.5		0		V
Maximum output voltage	Gain = 1.5		1.7		V
Minimum load resistance			50		kΩ
Maximum load capacitance			50		PF

3.3.5 Auxiliary Analog-to-Digital Converter

The auxiliary ADC is a 10-bit successive approximation A/D converter. The ADC has four input channels. Special offset cancellation is applied in the ADC.

Table 19: Performance of the auxiliary ADC.

Parameter	Conditions/Comments	Min.	Typ.	Max.	Unit
Resolution			10		bits
Integral non-linearity			±3		LSB
Differential non-linearity			±2		LSB
Number of input channels			5		
Analog input range	Without divider (e. g., ADC3)	0.1		1.2	V
	With divider	0.3		3.5	V
Conversion time				15	μs
Power up settling time				10	μs

3.3.6 LDO

SC6600D integrated low-voltage and low quiescent current low dropout regulators (LDO) for the internal power management purposes. Two more LDO regulators are designed for external use. All LDOs have their own bypass control signals. A 22 μF tantalum or MLCC ceramic capacitors are recommended for use with all the analog power LDOs, the digital core LDO and the two external LDOs.

Table 20: Performance of the integrated LDO regulators.

Parameter	Conditions/Comments	Min.	Typ.	Max.	Unit
LDO1					
Output voltage			2.85		V

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Parameter	Conditions/Comments	Min.	Typ.	Max.	Unit
Output current				100	mA
Output capacitor required for stability and ripple rejection		10		50	μF
LDO2					
Output voltage			2.8/1.8		V
Output current				50	mA
Output capacitor required for stability and ripple rejection		1		50	μF
LDO_VB					
Output voltage			2.8		V
Output current				10	mA
Output capacitor required for stability and ripple rejection		1		50	μF
LDO_VBO					
Output voltage			2.8		V
Output current				80	mA
Output capacitor required for stability and ripple rejection		10		50	μF
LDO_BB					
Output voltage			2.8		V
Output current				10	mA
Output capacitor required for stability and ripple rejection		1		50	μF
LDO_AUX					
Output voltage			2.8		V
Output current				10	mA
Output capacitor required for stability and ripple rejection		1		50	μF
LDO_PLL					
Output voltage			1.8/1.6/1.5/1.3		V
Output current				10	mA
Output capacitor required for stability and ripple rejection		1		50	μF
LDO for digital core					
Output voltage			1.8/1.6/1.5/1.3		V
Output current				100	mA
Output capacitor required for stability and ripple rejection		10		50	μF
LDO for VDDIO					
Output voltage			3.0/2.8/2.2/1.8		V
Output current				100	mA
Output capacitor required for stability and ripple rejection		10		50	μF
LDO for VMEM					
Output voltage			3.0/2.8/2.2/1.8		V
Output current				100	mA
Output capacitor required for stability and ripple rejection		10		50	μF
LDO for VSIM					
Output voltage			3.0/2.8/2.2/1.8		V
Output current				60	mA
Output capacitor required for stability and ripple rejection		1		50	μF

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4 Functional Description

This section provides detailed information about SC6600D functions, including description, control registers and software interface.

SC6600D has two general-purpose processors, ARM7TDMI MCU and TeakLite DSP. In general, the MCU and DSP control the operation of various ASIC hardware modules. The MCU or DSP prepares the data that needs the ASIC to process and sets up some control registers that tells the ASIC how to process the data. Therefore, the software control interface consists of data memories and control registers. The software interface sections define the organization of the data memories and the meanings of control register bits.

4.1 MCU Core and Internal Memories

The MCU sub-system is built on the ARM AMBA® bus structure. The internal memories and external memory interface are connected to the AHB bus, while other function blocks and peripheral interfaces are connected to the APB bus.

AMBA® is a registered trademark of Advanced RISC Machines Limited.

The core of the MCU subsystem is the ARM MCU core and its memories.

4.1.1 MCU Core

The micro-controller unit (MCU) used on SC6600D is ARM7TDMI from ARM Holdings. ARM7TDMI is a 32/16-bit RISC processor, a member of the ARM family of 32-bit microprocessors that offer high performance with very low power consumption and low gate count. ARM7TDMI works on instructions of 32 or 16 bits and data of 32, 16 or 8 bits. ARM7TDMI also provides in-circuit-emulation (ICE) for debugging purposes.

The embedded MCU runs a real-time operation system, performs the system control functions according to the GSM protocol stack, and services all peripheral components including man-machine interface.

4.1.2 MCU Internal SRAM

The MCU internal SRAM are configured as four parts, each having 16 KB (4 k words of 32 bits), with the option that some of them can be used on the DSP side. The internal SRAM can be read/written in 32, 16 or 8-bit operations.

4.1.3 MCU Internal ROM

The MCU internal ROM has 40 KB (10 k words of 32 bits). Part of the ROM is for boot/download purposes and others are for RTOS and other functions.

There is an option on the boot. With a boot control pin being high (default), the MCU will boot from the external FLASH. When the boot control pin is low, the MCU will boot from the internal ROM.

4.1.4 MCU Boot

The MCU can boot in two ways; one is from FLASH (the default) and the other from the internal ROM. When the system is first assembled the FLASH is empty, or when software upgrade is available the FLASH needs to be reloaded. In such cases, the system can be boot from the internal ROM. When boot from the internal ROM, program can be downloaded from the UART port to the FLASH. In normal operation, the system boot from the FLASH when powered on.

The boot mode switching is controlled at a strapping pin, PWMA (PA4). By default, this pin is pulled high at reset, defining the default boot mode. When needed, the pin can be pulled low at reset, switching to internal ROM boot.

The internal ROM boot supports boot from UART or NAND flash. The boot mode switching is controlled by two strapping pin, EMD15 and EMD14. By default these two pins are weakly pulled down in chip, so

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that the chip boots from UART0. Adding a pull up resistor on these two pins can switch to boot chip from a NAND flash. Refer to the following table.

Table 21: List of MCU boot options.

EMD15	EMD14	Boot-Mode Register Value	Boot Mode
-	-	0b00	UART0
-	Pulled up	0b01	NAND flash, 8-bit I/O, 3 address latch cycles
Pulled up	-	0b10	NAND flash, 16-bit I/O, 3 or 4 address latch cycles
Pulled up	Pulled up	0b11	NAND flash, 8-bit I/O, 3 address latch cycles

4.1.5 MCU Memory Address Map

On the MCU side, the address bus is 32-bit wide and the address map is presented in the following table. The MCU memory space can be remapped after reset.

Table 22: SC6600D MCU memory address map after reset.

Address Range	Memory Sector	Sub-Sector
0x0000_0000 – 0x0FFF_FFFF	External Memory/Internal Rom Space	When PA4 is pulled up, the MCU will boot from external Flash, and this address space is occupied by external memory: EMCS0: 0x00000000–0x03FFFFFF EMCS1: 0x04000000–0x07FFFFFF EMCS2: 0x08000000–0x0bFFFFFF EMCS3: 0x0c000000–0x0FFFFFFF When PA4 is pulled down, the MCU will boot from the internal ROM, and this address space is occupied by the internal ROM. Currently, 0x00000000 – 0x00004FFF is used. The first 2,560 bytes are boot code. Others are OS libraries, MP3 and MIDI libraries. PA4 is default to pull up and this space will be used as external memory space.
0x1000_0000 – 0x1FFF_FFFF	Internal Shared Memory Space	0x0000_0000 – 0x0000_1FFF is used.
0x2000_0000 – 0x200F_FFFF	External Memory Control registers Space	See Section 4.2.7 for details.
0x2010_0000 – 0x201F_FFFF	DMA Control registers Space	See Section 4.4.1 for details.
0x3000_0000 – 0x3FFF_FFFF	Internal Rom/External Memory (4 chip selects) Space	When PA4 is pulled down, this address space is occupied by external memory. When PA4 is pulled up, this address space is occupied by internal ROM. PA4 is default to pull up and this space will be used as internal ROM space
0x4000_0000 – 0x4FFF_FFFF	Internal On Chip RAM space	0x40000000 – 0x40003FFF 0x40004000 – 0x40007FFF 0x40008000 – 0x4000BFFF 0x4000C000 – 0x4000FFFF are the internal RAMs shared with DSP. The control bits for the shared RAM are bit 0 though bit 3 in the global register GEN2.
0x5000_0000 – 0x5FFF_FFFF	External Memory/Internal Rom Space	When PA4 is pulled up, this space is occupied by external memory: EMCS4: 0x50000000 – 0x53FFFFFF

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Address Range	Memory Sector	Sub-Sector
		EMCS5: 0x54000000 – 0x57FFFFFF EMCS6: 0x58000000 – 0x5BFFFFFF EMCS7: 0x5C000000 – 0x5FFFFFFF When PA4 is pulled down, this space is not accessible. PA4 is default to pull up and this space will be used as external memory space.
0x8000_0000 – 0x8FFF_FFFF	Peripheral Address Space	
	0x8000_0000	Interrupt Controller
	0x8100_0000	Timer/Counter
	0x8200_0000	RemPause
	0x8200_3000	Voice Band
	0x8300_0000	SERIAL0
	0x8400_0000	SERIAL1
	0x8500_0000	SIM
	0x8600_0000	I2C
	0x8700_0000	KPD
	0x8800_0000	PWM
	0x8900_0000	RTC
	0x8a00_0000	GPIO
	0x8b00_0000	GLB
	0x8c00_0000	Pin controls
	0x8d00_0000	GEA
	0x8e00_0000	SERIAL2
	0x8f00_0000	PCMCIA
0xC000_0000 – 0xDFFF_FFFF	ARM test Space	
Others	Undefined	

It should be noted that:

1. The re-map between the external memory and internal ROM can also be controlled by writing to 0x8200_0020 with 0x0000_0000 or 0x0000_0001. Writing with 0x0000_0000 corresponds to external memory starting from address 0x0000_0000 while writing with 0x0000_0001 corresponds to the internal ROM starting from address 0x0000_0000. The re-map completes in 4 clock cycles after the start of the above command.
2. For the internal shared memory, only 16-bit write and 8- or 16-bit read are supported. All Other memory accesses support byte, half word and word write/read.
3. Page mode and burst mode are supported for the flash memory read.

4.2 MCU External Memory Controller

SC6600D supports more external memories in addition to FLASH and SRAM. The external memory controller has the following features.

- It supports burst access mode for FLASH devices, in addition to the normal and page modes.
- It supports synchronous DRAM (SDRAM) at the maximum MCU speed with 0 wait state.
- It supports NAND FLASH memories.
- It supports a memory space up to 512 M bits (64 M bytes) for any single memory device (with [24:0] address bits, plus H/L selects).
- It provides eight chip-select (CS) pins.
- It supports both 1.8 V and 3.0 V memories.
- It supports another bus master to use the same memory bus.

4.2.1 MCU External Memory Interface

The external memory interface on the MCU side can support up to eight (8) external memory chips with up to 512 M bits (64 MB) each. When the memory system requires less chips or smaller sizes, some of the memory interface pins can be used for other purposes.

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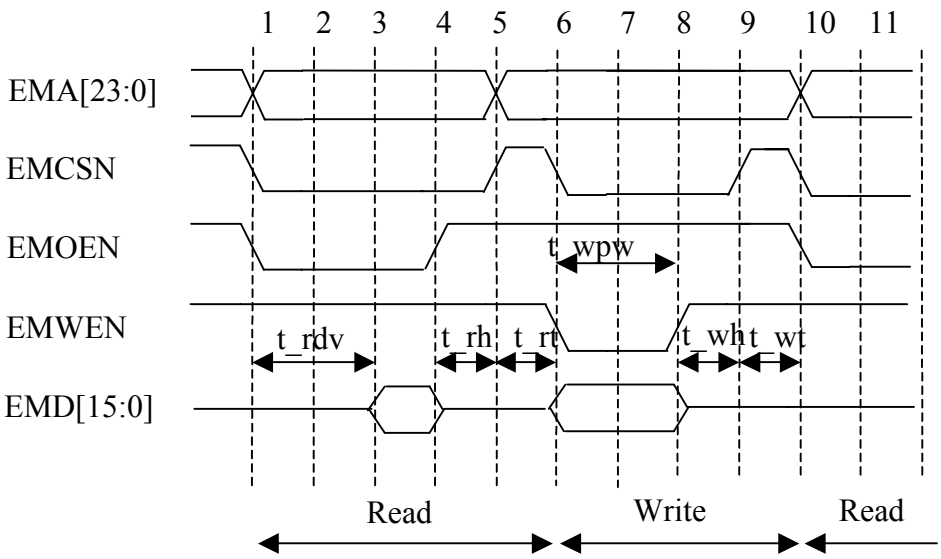
The external memory interface consists of the following pins.

- EMA [24:0], 25 address pins that can drive any single memory with a size of up to 64 MB (512 M bits). If smaller memories are used, EMA [24:22] can be used for other purposes.
- EMBL and EMBH, lower and upper byte selects. The data bus is 16-bit wide, and these two pins control which or both of the bytes are used.
- CLKMCU, MCU clock output. This can be used with synchronous memories or to monitor the on-chip MCU clock. For monitoring purposes, this pin can also be connected to three other internal clock signals.
- EMOE_N, output enable, active low.
- EMWE_N, write enable, active low.
- EMCS_N [7:0], 8 chip-select signals, and all are active low.
- EMD [15:0], external memory data bus.

SC6600D supports top boot FLASH devices and the FLASH chip can be of either Intel or AMD format.

4.2.2 External Memory Timing for a Single Access

Figure 7 shows the external memory timing for a single access. All the timing parameters can be programmed through control registers.



t_rdv : read data valid time
t_rh : read hold time
t_rt : read turnaround time
t_wpw : write pulse width
t_wh : write hold time
t_wt : write turnaround time

Figure 7: MCU external memory timing for a single access.

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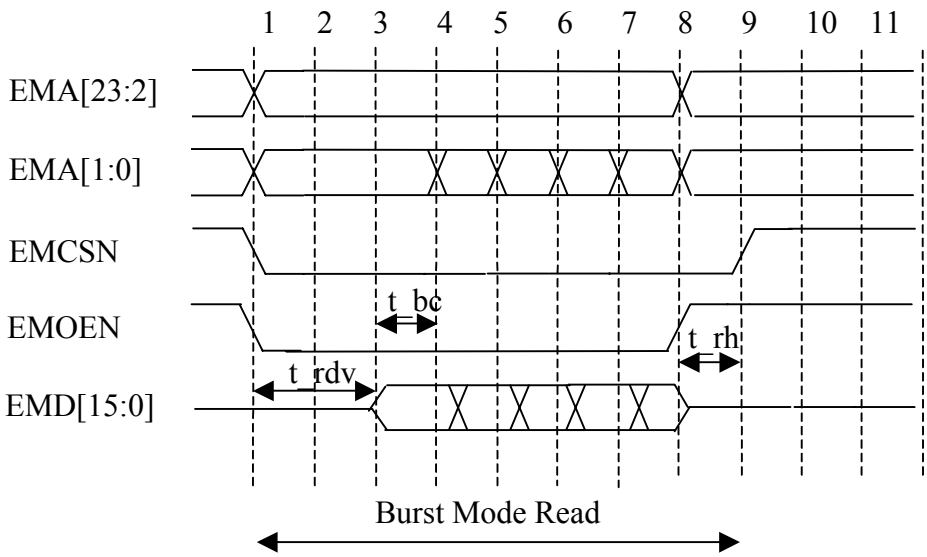
4.2.3 External Memory Timing for a Burst Access

Figure 8 shows the external memory timing for a burst access. All the timing parameters can be programmed through control registers.



t_rdv : read data valid time

t_rh : read hold time

t_bc : burst read cycle time. Can be set to 0 or 1

Figure 8: MCU external memory access for a burst access.

4.2.4 SDRAM Support

SC6600D can support synchronous DRAM (SDRAM) with 0 wait state.

4.2.5 NAND Flash Support

SC6600D can support NAND flash with the help of software.

4.2.6 Memory Bus Sharing

When the MCU on SC6600D is stopped, the external memory bus is in tri-state, allowing other devices to drive the bus.

4.2.7 External Memory Control Registers

Table 23: External memory control registers (base address: 0x2000_0000).

Address	Signal	Bit Pos	R/W	Default	Description
0x0000	ExtMemCtl0	[31:0]	R/W		
When bit 31 (SDRAM flag) is 0, the bit field definition is as follows.					
		[0]		0x1	Read to read turn around control
		[1]		0x1	Read to write turn around control
		[2]		0x1	Write to read turn around control
		[3]		0x1	Write to write turn around control
		[7:4]		0x1	First read data valid time under burst/page mode
		[11:8]		0x7	Read data valid time under normal mode
		[15:12]		0x7	Write pulse width
		[16]		0x1	Read hold time

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Address	Signal	Bit Pos	R/W	Default	Description
		[17]		0x1	Write hold time
		[19:18		0x3	Second and following read data valid time under page mode
		[21]		0x0	Page mode flag
		[22]		0x0	Burst mode flag
		[26]		0x0	Flash
		[24]		0x1	Not use buffer in the external memory control module
		[25]		0x0	Write protection flag
		[27]		0	Bus error indicator
		[30]		0	Write protect error indicator
		[31]		0x1	SDRAM flag
When bit 31 (SDRAM flag) is 1, the bit field definition is as follows.					
		[3:0]			Refresh period time
		[7:4]			Precharge period time
		[10:8]			Active to read/write time
		[12:11]			Write recovery time
		[14:13]			CAS latency. Can be set to 2 or 3.
		[17:15]			Burst length control. Set to burst of 8 under normal condition (0x011). Set to full page under DCAM write mode (0x111).
		[18]			Control the mapping of SDRAM address to AHB address: 0: (row_address, bank_address, col_address) map to AHB address (MSB to bit1). 1: (bank address, row_address, col_address) map to AHB address (MSB to bit1).
		[20:19]			The size of the SDRAM. 00: 4Mx16, 01: 8Mx16, 10:16Mx16.
		[30]			Write protection flag
		[27]			Bus error indicator
		[28]			Write protect error indicator
		[31]			SDRAM flag
0x0004	ExtMemCtl1	[31:0]	R/W		Per bit definition and default values are the same as ExtMemCtl0.
0x0008	ExtMemCtl2	[31:0]	R/W		Per bit definition and default values are the same as ExtMemCtl0.
0x000C	ExtMemCtl3	[31:0]	R/W		Per bit definition and default values are the same as ExtMemCtl0.
0x0010	ExtMemCtl4	[31:0]	R/W		Per bit definition and default values are the same as ExtMemCtl0.
0x0014	ExtMemCtl5	[31:0]	R/W		Per bit definition and default values are the same as ExtMemCtl0.
0x0018	ExtMemCtl6	[31:0]	R/W		Per bit definition and default values are the same as ExtMemCtl0.
0x001C	ExtMemCtl7	[31:0]	R/W		Per bit definition and default values are the same as ExtMemCtl0.
0x0020	ExtMemINI	[31:0]	R/W		External memory initialization control
		[4:0]		0	Extended mode register load value
		[10:0]		0	DCAM write data total number
		[13:11]		0	Refresh interval control
		[21:14]		0	Refresh prescale value
		[22]		0	Initial mode register request
		[23]		0	Load mode register request

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Address	Signal	Bit Pos	R/W	Default	Description
		[24]		0	Load extended mode register request
		[25]		0	Suspension request
		[26]		0	Resume request
		[29:27]		0	Indicate the ExtMemCtlN number used in initial process.
		[30]		0	DCAM data write request
		[31]		0	Force buffer flush

Note:

- For all the ExtMemCtl registers, the bit field definition is exactly the same.
- Correct programming of ExtMemCtl registers based on the system configuration is needed to make the system work properly.
- ExtMemCtl0 to ExtMemCtl7 correspond to CSN0 to CSN7, respectively.
- Please refer to flash/SRAM/SDRAM data sheet for more info on read write timing.

4.3 MCU Memory Remap and MCU Stop

4.3.1 MCU Stop

The MCU can be stopped independently, when it is not doing any operation for power saving.

4.3.2 MCU Memory Remap

The MCU memory space can be remapped. This controls the MCU starting point, either from the internal ROM or from an external memory at CSN0.

4.3.3 Remap and Pause Control Registers

Table 24: Remap and pause control registers (base address: 0x8200_0000).

Address	Signal	Bit Pos	R/W	Default	Description
0x0000	MCU_STOP	[15:0]	W only	0	Writing any value to this register will STOP the MCU and the HBUS. The MCU will come out of the STOP state when any interrupt is received.
0x0020	Remap	[15:0]	R/W		Remap control
		[0]		0	Power strapped in. Writing 0 to this bit maps external memory to 0x00000000. Writing 1 to this bit maps the internal ROM to 0x00000000.

4.4 MCU Bus DMA

SC6600D provides an eight-channel DMA for faster data transfer.

4.4.1 MCU Bus DMA Control Registers

Table 25: DMA control registers (base address: 0x2010_0000).

Address	Signal	Bit Pos	R/W	Default	Description
0x0000	General Control Register	[31:0]	R/W		
		[31:16]		0	Control the interval between the data transfer burst. The unit is bus clock. Two consecutive bursts will be separate by an interval defined by this parameter.
		[15:2]		0	Reserved.

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Address	Signal	Bit Pos	R/W	Default	Description
		[1]			Error abort enable.
		[0]			pause_req.
0x0004	Channel 0 to 7 interrupt enable register	[31:0]	R/W	0	
		[7:0]			Channel 0 to channel 7 interrupt enable.
0x0020	Channel 0 config	[15:0]	R/W		
		[0]		0	Channel enable (channel data transfer start)
		[4:1]			Reserved.
		[5]			Hardware request enable
		[7]			Link list pointer enable
		[10]			Channel busy.
		[11]			Data transfer done
		[12]			Data transfer error.
		[15:13]			Channel data transfer priority.
		[16]			Channel error interrupt enable
		[17]			Total size data transferred interrupt enable
		[18]			Burst size data transferred interrupt enable
		[19]			Channel error interrupt request bit; The actual interrupt request equals
		[20]			Total size data transferred interrupt request bit
		[21]			Burst size data transferred interrupt request bit
0x0024	Channel 0 size ctl	[31:0]	R/W		
		[11:0]		0	Total data transfer size.
		[15]		0	Infinite data transfer enable.
		[24:16]		0	Burst size.
		[27:25]			Reserved.
		[29:28]		0	Data transfer size. 00: byte. 01: half word. 10: word.
		[30]		0	Destination data address increase in data transfer.
		[31]		0	Source address increase in data transfer.
0x0028	Channel 0 source address	[31:0]	R/W		Source address
0x002C	Channel 0 destination address	[31:0]	R/W		Destination address
0x0030	Channel 0 link list pointer register	[31:0]	R/W		Link list pointer address
0x0040	Channel 1 config	[15:0]	R/W		
		[0]		0	Channel enable (channel data transfer start)
		[4:1]			Reserved.

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Address	Signal	Bit Pos	R/W	Default	Description
		[5]			Hardware request enable
		[7]			Link list pointer enable
		[10]			Channel busy.
		[11]			Data transfer done
		[12]			Data transfer error.
		[15:13]			Channel data transfer priority.
		[16]			Channel error interrupt enable
		[17]			Total size data transferred interrupt enable
		[18]			Burst size data transferred interrupt enable
		[19]			Channel error interrupt request bit; The actual interrupt request equals
		[20]			Total size data transferred interrupt request bit
		[21]			Burst size data transferred interrupt request bit
0x0044	Channel 1 size ctl	[31:0]	R/W		
		[11:0]		0	Total data transfer size.
		[15]		0	Infinite data transfer enable.
		[24:16]		0	Burst size.
		[27:25]			Reserved.
		[29:28]		0	Data transfer size. 00: byte. 01: half word. 10: word.
		[30]		0	Destination data address increase in data transfer.
		[31]		0	Source address increase in data transfer.
0x0048	Channel 1source address	[31:0]	R/W		Source address
0x004C	Channel 1 destination address	[31:0]	R/W		Destination address
0x0050	Channel1 link list pointer register	[31:0]	R/W		Link list pointer address
0x0060	Channel 2 config	[15:0]	R/W		
		[0]		0	Channel enable (channel data transfer start)
		[4:1]			Reserved.
		[5]			Hardware request enable
		[7]			Link list pointer enable
		[10]			Channel busy.
		[11]			Data transfer done
		[12]			Data transfer error.
		[15:13]			Channel data transfer priority.
		[16]			Channel error interrupt enable
		[17]			Total size data transferred interrupt enable
		[18]			Burst size data transferred interrupt enable
		[19]			Channel error interrupt request bit;

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Address	Signal	Bit Pos	R/W	Default	Description
					The actual interrupt request equals
		[20]			Total size data transferred interrupt request bit
		[21]			Burst size data transferred interrupt request bit
0x0064	Channel 2 size ctl	[31:0]	R/W		
		[11:0]		0	Total data transfer size.
		[15]		0	Infinite data transfer enable.
		[24:16]		0	Burst size.
		[27:25]			Reserved.
		[29:28]		0	Data transfer size. 00: byte. 01: half word. 10: word.
		[30]		0	Destination data address increase in data transfer.
		[31]		0	Source address increase in data transfer.
0x0068	Channel 2 source address	[31:0]	R/W		Source address
0x006C	Channel2 destination address	[31:0]	R/W		Destination address
0x0070	Channel 2 link list pointer register	[31:0]	R/W		Link list pointer address
0x0080	Channel 3 config	[15:0]	R/W		
		[0]		0	Channel enable (channel data transfer start)
		[4:1]			Reserved.
		[5]			Hardware request enable
		[7]			Link list pointer enable
		[10]			Channel busy.
		[11]			Data transfer done
		[12]			Data transfer error.
		[15:13]			Channel data transfer priority.
		[16]			Channel error interrupt enable
		[17]			Total size data transferred interrupt enable
		[18]			Burst size data transferred interrupt enable
		[19]			Channel error interrupt request bit; The actual interrupt request equals
		[20]			Total size data transferred interrupt request bit
		[21]			Burst size data transferred interrupt request bit
0x0084	Channel 3 size ctl	[31:0]	R/W		
		[11:0]		0	Total data transfer size.
		[15]		0	Infinite data transfer enable.
		[24:16]		0	Burst size.
		[27:25]			Reserved.
		[29:28]		0	Data transfer size.

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Address	Signal	Bit Pos	R/W	Default	Description
					00: byte. 01: half word. 10: word.
		[30]		0	Destination data address increase in data transfer.
		[31]		0	Source address increase in data transfer.
0x0088	Channel 3 source address	[31:0]	R/W		Source address
0x008C	Channel 3 destination address	[31:0]	R/W		Destination address
0x0090	Channel 3 link list pointer register	[31:0]	R/W		Link list pointer address
0x00A0	Channel 4 config	[15:0]	R/W		
		[0]		0	Channel enable (channel data transfer start)
		[4:1]			Reserved.
		[5]			Hardware request enable
		[7]			Link list pointer enable
		[10]			Channel busy.
		[11]			Data transfer done
		[12]			Data transfer error.
		[15:13]			Channel data transfer priority.
		[16]			Channel error interrupt enable
		[17]			Total size data transferred interrupt enable
		[18]			Burst size data transferred interrupt enable
		[19]			Channel error interrupt request bit; The actual interrupt request equals
		[20]			Total size data transferred interrupt request bit
		[21]			Burst size data transferred interrupt request bit
0x00a4	Channel 4 size ctl	[31:0]	R/W		
		[11:0]		0	Total data transfer size.
		[15]		0	Infinite data transfer enable.
		[24:16]		0	Burst size.
		[27:25]			Reserved.
		[29:28]		0	Data transfer size. 00: byte. 01: half word. 10: word.
		[30]		0	Destination data address increase in data transfer.
		[31]		0	Source address increase in data transfer.
0x00a8	Channel 4 source address	[31:0]	R/W		Source address
0x00aC	Channel 4 destination address	[31:0]	R/W		Destination address

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Address	Signal	Bit Pos	R/W	Default	Description
0x00b0	Channel 4 link list pointer register	[31:0]	R/W		Link list pointer address
0x00c0	Channel 5 config	[15:0]	R/W		
		[0]		0	Channel enable (channel data transfer start)
		[4:1]			Reserved.
		[5]			Hardware request enable
		[7]			Link list pointer enable
		[10]			Channel busy.
		[11]			Data transfer done
		[12]			Data transfer error.
		[15:13]			Channel data transfer priority.
		[16]			Channel error interrupt enable
		[17]			Total size data transferred interrupt enable
		[18]			Burst size data transferred interrupt enable
		[19]			Channel error interrupt request bit; The actual interrupt request equals
		[20]			Total size data transferred interrupt request bit
		[21]			Burst size data transferred interrupt request bit
0x00c4	Channel 5 size ctl	[31:0]	R/W		
		[11:0]		0	Total data transfer size.
		[15]		0	Infinite data transfer enable.
		[24:16]		0	Burst size.
		[27:25]			Reserved.
		[29:28]		0	Data transfer size. 00: byte. 01: half word. 10: word.
		[30]		0	Destination data address increase in data transfer.
		[31]		0	Source address increase in data transfer.
0x00c8	Channel 5 source address	[31:0]	R/W		Source address
0x00CC	Channel 5 destination address	[31:0]	R/W		Destination address
0x00D0	Channel 5 link list pointer register	[31:0]	R/W		Link list pointer address
0x00E0	Channel 6 config	[15:0]	R/W		
		[0]		0	Channel enable (channel data transfer start)
		[4:1]			Reserved.
		[5]			Hardware request enable
		[7]			Link list pointer enable
		[10]			Channel busy.
		[11]			Data transfer done
		[12]			Data transfer error.

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Address	Signal	Bit Pos	R/W	Default	Description
		[15:13]			Channel data transfer priority.
		[16]			Channel error interrupt enable
		[17]			Total size data transferred interrupt enable
		[18]			Burst size data transferred interrupt enable
		[19]			Channel error interrupt request bit; The actual interrupt request equals
		[20]			Total size data transferred interrupt request bit
		[21]			Burst size data transferred interrupt request bit
0x00E4	Channel 6 size ctl	[31:0]	R/W		
		[11:0]		0	Total data transfer size.
		[15]		0	Infinite data transfer enable.
		[24:16]		0	Burst size.
		[27:25]			Reserved.
		[29:28]		0	Data transfer size. 00: byte. 01: half word. 10: word.
		[30]		0	Destination data address increase in data transfer.
		[31]		0	Source address increase in data transfer.
0x00E8	Channel 6 source address	[31:0]	R/W		Source address
0x00EC	Channel 6 destination address	[31:0]	R/W		Destination address
0x00F0	Channel 6 link list pointer register	[31:0]	R/W		Link list pointer address
0x0100	Channel 7 config	[15:0]	R/W		
		[0]		0	Channel enable (channel data transfer start)
		[4:1]			Reserved.
		[5]			Hardware request enable
		[7]			Link list pointer enable
		[10]			Channel busy.
		[11]			Data transfer done
		[12]			Data transfer error.
		[15:13]			Channel data transfer priority.
		[16]			Channel error interrupt enable
		[17]			Total size data transferred interrupt enable
		[18]			Burst size data transferred interrupt enable
		[19]			Channel error interrupt request bit; The actual interrupt request equals
		[20]			Total size data transferred interrupt request bit
		[21]			Burst size data transferred interrupt request bit

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Address	Signal	Bit Pos	R/W	Default	Description
0x0104	Channel 7 size ctl	[31:0]	R/W		
		[11:0]		0	Total data transfer size.
		[15]		0	Infinite data transfer enable.
		[24:16]		0	Burst size.
		[27:25]			Reserved.
		[29:28]		0	Data transfer size. 00: byte. 01: half word. 10: word.
		[30]		0	Destination data address increase in data transfer.
		[31]		0	Source address increase in data transfer.
0x0108	Channel 7 source address	[31:0]	R/W		Source address
0x010C	Channel 7 destination address	[31:0]	R/W		Destination address
0x0110	Channel 7 link list pointer register	[31:0]	R/W		Link list pointer address

4.5 MCU Bus Monitor

SC6600D provides an MCU bus monitor for software debug and ROM code patch. When the MCU reads a specific data from a specific address or writes a specific data to a specific address an interrupt is triggered. In other words, the following conditions can trigger an interrupt.

- Access a specific address (either read or write).
- Read a specific data from a specific address.
- Write a specific data to a specific address.

4.5.1 Bus Monitor Control Registers

Table 26: Bus monitor control registers (base address: 0x2000_0000).

Address	Signal	Bit Pos	R/W	Default	Description
0x0028	Bm_addr0	[31:0]	R/W		Address for bus monitor point 0
0x002C	Bm_addr0_msk	[31:0]	R/W		Address mask for bus monitor point 0
0x0030	Bm_rdata0	[31:0]	R/W		Read data for bus monitor point 0
0x0034	Bm_rdata0_msk	[31:0]	R/W		Read data mask for bus monitor point 0
0x0038	Bm_wdata0	[31:0]	R/W		Write data for bus monitor point 0
0x003C	Bm_wdata0_msk	[31:0]	R/W		Write data mask for bus monitor point 0
0x0040	Bm_addr1	[31:0]	R/W		Address for bus monitor point 1
0x0044	Bm_addr1_msk	[31:0]	R/W		Address mask for bus monitor point 1
0x0048	Bm_rdata1	[31:0]	R/W		Read data for bus monitor point 1
0x004C	Bm_rdata1_msk	[31:0]	R/W		Read data mask for bus monitor point 1
0x0050	Bm_wdata1	[31:0]	R/W		Write data for bus monitor point 1
0x0054	Bm_wdata1_msk	[31:0]	R/W		Write data mask for bus monitor point 1
0x0058	Bm_addr2	[31:0]	R/W		Address for bus monitor point 2
0x005C	Bm_addr2_msk	[31:0]	R/W		Address mask for bus monitor point 2
0x0060	Bm_rdata2	[31:0]	R/W		Read data for bus monitor point 2
0x0064	Bm_rdata2_msk	[31:0]	R/W		Read data mask for bus monitor point 2
0x0068	Bm_wdata2	[31:0]	R/W		Write data for bus monitor point 2
0x006C	Bm_wdata2_msk	[31:0]	R/W		Write data mask for bus monitor point 2

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Address	Signal	Bit Pos	R/W	Default	Description
0x0070	Bm_addr3	[31:0]	R/W		Address for bus monitor point 3
0x0074	Bm_addr3_msk	[31:0]	R/W		Address mask for bus monitor point 3
0x0078	Bm_rdata3	[31:0]	R/W		Read data for bus monitor point 3
0x007C	Bm_rdata3_msk	[31:0]	R/W		Read data mask for bus monitor point 3
0x0080	Bm_wdata3	[31:0]	R/W		Write data for bus monitor point 3
0x0084	Bm_wdata3_msk	[31:0]	R/W		Write data mask for bus monitor point 3
0x0088	Bm_addr4	[31:0]	R/W		Address for bus monitor point 4
0x008C	Bm_addr4_msk	[31:0]	R/W		Address mask for bus monitor point 4
0x0090	Bm_rdata4	[31:0]	R/W		Read data for bus monitor point 4
0x0094	Bm_rdata4_msk	[31:0]	R/W		Read data mask for bus monitor point 4
0x0098	Bm_wdata4	[31:0]	R/W		Write data for bus monitor point 4
0x009C	Bm_wdata4_msk	[31:0]	R/W		Write data mask for bus monitor point 4
0x00a0	Bm_addr5	[31:0]	R/W		Address for bus monitor point 5
0x00a4	Bm_addr5_msk	[31:0]	R/W		Address mask for bus monitor point 5
0x00a8	Bm_rdata5	[31:0]	R/W		Read data for bus monitor point 5
0x00aC	Bm_rdata5_msk	[31:0]	R/W		Read data mask for bus monitor point 5
0x00b0	Bm_wdata5	[31:0]	R/W		Write data for bus monitor point 5
0x00b4	Bm_wdata5_msk	[31:0]	R/W		Write data mask for bus monitor point 5
0x00b8	Bm_addr6	[31:0]	R/W		Address for bus monitor point 6
0x00bC	Bm_addr6_msk	[31:0]	R/W		Address mask for bus monitor point 6
0x00C0	Bm_rdata6	[31:0]	R/W		Read data for bus monitor point 6
0x00C4	Bm_rdata6_msk	[31:0]	R/W		Read data mask for bus monitor point 6
0x00C8	Bm_wdata6	[31:0]	R/W		Write data for bus monitor point 6
0x00CC	Bm_wdata6_msk	[31:0]	R/W		Write data mask for bus monitor point 6
0x00D0	Bm_addr7	[31:0]	R/W		Address for bus monitor point 7
0x00D4	Bm_addr7_msk	[31:0]	R/W		Address mask for bus monitor point 7
0x00D8	Bm_rdata7	[31:0]	R/W		Read data for bus monitor point 7
0x00DC	Bm_rdata7_msk	[31:0]	R/W		Read data mask for bus monitor point 7
0x00E0	Bm_wdata7	[31:0]	R/W		Write data for bus monitor point 7
0x00E4	Bm_wdata7_msk	[31:0]	R/W		Write data mask for bus monitor point 7
0x00E8	Bm_size	[31:0]	R/W		Size for bus monitor point 0 – 7
		[2:0]		0	Size for bus monitor point 0
		[3]		0	Reserved
		[6:4]		0	Size for bus monitor point 1
		[7]		0	Reserved
		[10:8]		0	Size for bus monitor point 2
		[11]		0	Reserved
		[14:12]		0	Size for bus monitor point 3
		[15]		0	Reserved
		[18:16]		0	Size for bus monitor point 4
		[19]		0	Reserved
		[22:20]		0	Size for bus monitor point 5
		[23]		0	Reserved
		[26:24]		0	Size for bus monitor point 6
		[27]		0	Reserved
		[30:28]		0	Size for bus monitor point 7
		[31]		0	Reserved
0x00EC	Bm_size mask	[31:0]	R/W		Size mask for bus monitor point 0 - 7
		[2:0]		0	Size mask for bus monitor point 0
		[3]		0	Reserved
		[6:4]		0	Size mask for bus monitor point 1
		[7]		0	Reserved
		[10:8]		0	Size mask for bus monitor point 2
		[11]		0	Reserved
		[14:12]		0	Size mask for bus monitor point 3

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Address	Signal	Bit Pos	R/W	Default	Description
		[15]		0	Reserved
		[18:16]		0	Size mask for bus monitor point 4
		[19]		0	Reserved
		[22:20]		0	Size mask for bus monitor point 5
		[23]		0	Reserved
		[26:24]		0	Size mask for bus monitor point 6
		[27]		0	Reserved
		[30:28]		0	Size mask for bus monitor point 7
		[31]		0	Reserved
0x00F0	Bm_ctl	[31:0]	R/W		Monitor control bits for point 0 - 7
		[1:0]		0	Control for point 0: 00: disabled 01: compare write data 10: compare read data 11: compare both R/W
		[3:2]		0	Control for point 1, and the bit definition is the same as the control for point 0.
		[5:4]		0	Control for point 2, and the bit definition is the same as the control for point 0.
		[7:6]		0	Control for point 3, and the bit definition is the same as the control for point 0.
		[9:8]		0	Control for point 4, and the bit definition is the same as the control for point 0.
		[11:10]		0	Control for point 5, and the bit definition is the same as the control for point 0.
		[13:12]		0	Control for point 6, and the bit definition is the same as the control for point 0.
		[15:14]		0	Control for point 7, and the bit definition is the same as the control for point 0.
		[16]		0	Bus monitor enable

4.6 MCU Interrupt Controller

The MCU interrupt controller collects interrupt trigger signals, applies mask on them and generates one of the MCU interrupt signals, FIQ or IRQ (Figure 9). The interrupt triggers can be programmed to be either level sensitive or edge sensitive, triggered either at high-level or at low-level in level-sensitive case, either at positive edge or at negative edge in edge-triggered mode.

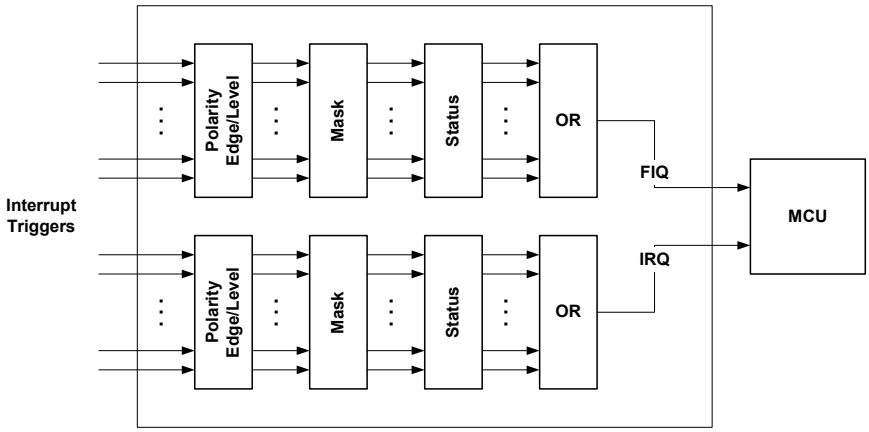

Figure 9: MCU interrupt controller.

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4.6.1 Interrupt Control Registers

Table 27: MCU Interrupt control registers (base address: 0x8000_0000).

Address	Signal	Bit Pos	R/W	Default	Description
0x0000	Irq_status	[31:0]	R only	0	Interrupt status after masked by irq_enable register.
	Uart_sleep_Int	0		0	UART RX pin I/O Interrupt detected during PLL power down
	Soft_int	1		0	Software int bit
	COMMRX	2		0	Interrupt from ARM comm. Rx
	COMMTX	3		0	Interrupt from ARM comm. Tx
	INTCNT1	4		0	Timer 1 interrupt
	INTCNT2	5		0	Timer 2 interrupt
	Gpio_irq	6		0	Interrupt from GPIO including CHINT. All GPIOs have polarity control.
	Rtc_irq	7		0	Interrupt from real time clock
	Kpd_irq	8		0	Interrupt from keypad
	I2c_irq	9		0	Interrupt from 2ws
	Sim_irq	10		0	Interrupt from SIM
	Ser_irq0	11		0	Serial port 0 interrupt
	Ser_irq1	12		0	Serial port 1 interrupt
	Dsp_irq	13		0	Interrupt from DSP
	Adc_irq	14		0	ADC done interrupt
	Gea_poll_int	15		0	GEA done interrupt
	Syst_int	16		0	Interrupt from System 1 ms timer
	Pcm_irq	17		0	Interrupt from PCMCIA
	Ser_irq2	18		0	Serial port 2 interrupt
	spk_irq	19		0	Speaker interrupt
	Dma_irq	20		0	DMA interrupt
	Vbc_irq	21		0	Voice Band interrupt
	bmon_irq0	22		0	Bus monitor 0 interrupt
	bmon_irq1	23		0	Bus monitor 1 interrupt
	bmon_irq2	24		0	Bus monitor 2 interrupt
	bmon_irq3	25		0	Bus monitor 3 interrupt
	bmon_irq4	26		0	Bus monitor 4 interrupt
	bmon_irq5	27		0	Bus monitor 5 interrupt
	bmon_irq6	28		0	Bus monitor 6 interrupt
	bmon_irq7	29		0	Bus monitor 7 interrupt
	Wdg_irq	30		0	Watchdog interrupt
	PBINT	31		0	PBINT interrupt
0x0004	Irq_rawstatus	[31:0]	R only	0	Raw interrupt status from different interrupt source. Per bit definition is the same as Irq_status register.
0x0008	Irq_enable	[31:0]	R/W	0	Enable bits for the corresponding interrupt sources. Write to this register with corresponding bits set to 1 enables the corresponding interrupts. Per bit definition is the same as Irq_status register.
0x000C	Irq_disable	[31:0]	W only	0	Write to this register with corresponding bits set to 1 disables the corresponding interrupts. Per bit definition is the same as Irq_status register.
0x0010	Irq_soft	[1]	W only	0	Write to this register bit will set the soft_irq with the value in write data bit 1.
0x0014	Irq_test_src	[31:0]	R/W	0	Test mode source interrupt generation. Per bit definition is the same as Irq_status

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Address	Signal	Bit Pos	R/W	Default	Description
					register.
0x0018	Irq_test_sel	[0]	R/W	0	When this bit is set, IRQ interrupts generate from Irq_test_src test register.
0x001C	Uint_status	[8:0]	R only	0	UART I/O pin Interrupt raw status. The interrupt detection catches any level change of 9 UART RX lines from I/O pins in sleep mode. Interrupt bit definition: Bit 8: UART_CTSN2 Bit 7: UART_DSRN2 Bit 6: UART_RXD2 Bit 5: UART_CTSN1 Bit 4: UART_DSRN1 Bit 3: UART_RXD1 Bit 2: UART_CTSN0 Bit 1: UART_DSRN0 Bit 0: UART_RXD0
0x0020	Fiq_status	[31:0]	R only	0	FIQ Interrupt status masked. FIQ shares the same interrupt sources as IRQ seen above.
0x0024	Fiq_rawstatus	[31:0]	R only	0	FIQ Interrupt status raw.
0x0028	Fiq_enable	[31:0]	R/W	0	Enable bit for the FIQ interrupt sources. Write to this register with bit 0 set to 1 enables the FIQ interrupts.
0x002C	Fiq_disable	[31:0]	W only	0	Write to this register with bit 0 set to 1 disables the FIQ interrupts
0x0030	Fiq_soft	[1]	W only	0	Write to this register bit will set the soft_fiq with the value in write data bit 1.
0x0034	Fiq_test_src	[31:0]	R/W	0	Test mode source interrupt generation. Per bit definition is the same as fiq_status register.
0x0038	Fiq_test_sel	[0]	R/W	0	When this bit is set, Fiq interrupts generate from fiq_test_src test register.
0x003C	Uint_en	[8:0]	R/W	0	UART I/O pin interrupt mask
	Uint_clr	[15]	R/W	0	When this bit is set, all Uint_status bits are cleared.
	unit_pol	[24:16]	R/W	0	Polarity control bits correspond to 9 UART I/O interrupt sources. If set, the related interrupt bit is inverted.

4.7 MCU Timers

SC6600D provides several timers at the MCU side.

4.7.1 General-Purpose Timers

The MCU sub-system provides two general-purpose timers. These two timers can be controlled individually.

Each timer has a 22-bit counter and the stop count (one shot mode) or period count (periodical mode) can be set to a control register. The frequency of the count clock is 32.768 kHz. As a result, the longest time interval is about 128 second.

At the end of the count, the timer can generate an interrupt to the MCU.

4.7.1.1 Timer Control Registers

Table 28: Timer control registers (base address: 0x8100_0000).

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Address	Signal	Bit Pos	R/W	Default	Description
0x0000	Timer0_load	[21:0]	R/W	0	Write to this register will reload the timer with the new value.
0x0004	Timer0_value	[21:0]	R only	0	Return the current timer value.
0x0008	Timer0_control	[7:0]	W only	0	Timer control.
		[3:2]		0	Reserved.
		[6]		0	Mode control 1: select periodic mode 0: select free running mode
		[7]		0	Enable bit of this timer.
0x000C	Timer0_clear	[15:0]	W only	0	Write to this register will clear the interrupt generated by this timer.
0x0020	Timer1_load	[21:0]	R/W	0	Write to this register will reload the timer with the new value.
0x0024	Timer1_value	[21:0]	R only	0	Return the current timer value.
0x0028	Timer1_control	[15:0]	W only	0	Timer control.
		[3:2]		0	Reserved.
		[6]		0	Mode control 1: select periodic mode 0: select free running mode
		[7]		0	Enable bit of this timer.
0x002C	Timer1_clear	[15:0]	W only	0	Write to this register will clear the interrupt generated by this timer.

4.7.2 32-bit System Counter

The system counter is a free-running counter and it counts whenever the RTC clock is running. The counter gets reset to zero at the hardware reset.

When the system counter count equals to the value of SYST_ALM register (system counter alarm, at 0x8B00_0040), an interrupt is generated. The interrupt length is one cycle of the RTC clock, or about 30.5 µs at 32.768 kHz. Before sent to the MCU, the rising edge of this interrupt is latched by RTC clock, the interrupt status shows on register sys_ctl bit [1]. The MCU is able to clear it through register sys_ctl bit [3].

4.7.2.1 32-bit System Counter Registers

Table 29: 32-bit system counter registers (base address: 0x8700_0000).

Address	Signal	Bit Pos	R/W	Default	Description
0x001C	System_count0	[31:0]	R only		The 32 bit system counter
0x0020	Unused	[15:0]			Reserved.
0x0024	Sys_ctl				
	Syst_int_en	[0]	R/W		System timer interrupt enable
	Syst_int_status	[1]	R only		System timer interrupt status
		[2]	R only		System timer interrupt value
	Syst_int_iclr	[3]	W only		Write 1 to this bit will clear the System timer interrupt status bit

Please note:

- The tick of the system counter is selected by bit 14 of the global register GEN1 (address 0x8B00_0018). Please refer to the global register section.
- There is no shadow register anymore; the MCU needs to read twice to ensure the system counter value being read is correct.

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4.7.3 Watchdog Timer

SC6600D provides a watchdog timer (WDT) that can reset the MCU subsystem if the MCU SW does not reload the timer. The timer has 32 bits.

The counter is controlled by RTC clock. With RTC clock at 32.768 kHz, 32 bits provide up to 131,072 seconds or more than 36 hours of count time.

The watchdog works in one of the following modes:

- The counter counts down to 0 and then sends an interrupt to the MCU.
- The counter counts down to 0 and then reset the MCU subsystem.

The watchdog after HW reset is disabled by default.

The control registers in WDT are controlled by a lock and only a specific value can unlock the register write enable.

4.7.3.1 Watchdog Timer Registers (0x8900_3000)

Table 30: Watchdog timer registers (base address: 0x8900_0300).

Address	Signal	Bit Pos	R/W	Default	Description
0x0000	Load	[31:0]	R/W	0x0003_FFFF	Watch dog Load (default 8 seconds) The unit of this load value is rtc_clk cycles.
0x0004	Value	[31:0]	R only	0xFFFF_FFFF	Current value for watch dog counter
0x0008	Control	[31:0]	R/W	2	Watch dog control register
		[0]		0	Watch dog interrupt mode enable
		[1]		1	Watch dog rtc_clk gating control 0: no rtc_clk to drive the counter. 1: counter is driven by rtc_clk.
0x000C	Interrupt Clear	[31:0]	W only	-	Write any value into this register clear the watch dog interrupt
0x0010	Raw interrupt	[0]	R only	0	Raw watch dog interrupt
0x0014	Masked interrupt	[0]	R only	0	Masked watch dog interrupt
0x0C00	Lock Register	[31:0]	W only	-	Write 0x1ACCE551: unlock Write others: lock
		[0]	R only	0	1'b0: unlocked 1'b1: locked

4.8 MCU Peripherals

Many peripheral control functions are provided for easy system integration.

Most of the peripherals are controlled by the MCU, including data ports, SIM interface, keypad interface, etc. The data ports are provided for data transfers with other devices, and they include both serial ports (UART and 2-wire serial interface) and a parallel port.

The MCU control registers are listed with the functional modules. Only 32 bits read and write are supported for control register access.

4.8.1 UART Controller

SC6600D provides three UART ports, UART0 is on the MCU side, and UART1 and UART2 can be used on either the MCU or the DSP side.

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4.8.1.1 Overview

SC6600D's universal asynchronous receiver/transmitter (UART) serial interfaces are compatible to National 16550 or Intel 8251 asynchronous serial interface. Following are the features the UART interfaces provide:

- Full-duplex operation.
- Hardware flow control support.
- Support full modem hand-shaking signals.
- 128 byte of Rx FIFO and 128 byte of Tx FIFO.

Each UART in SC6600D shares the same design and has an independent baud rate generator, which is used as a clock reference for data recovery. Each of them also has a 128-byte Rx FIFO and a 128-byte Tx FIFO to decrease MCU interrupt load during the data receiving or transmitting. In the text that follows, only the register and signal names of the UART0 are used. All of these references apply to UART1 and UART2 as well.

4.8.1.2 Functional Description

Each UART includes the pins as shown in the following table.

Table 31: List of UART pins.

Pin Name	Signal	I/O	Description
U0TXD	Transmit data	O	Transmit data output.
U0RXD	Receive data	I	Receive data input.
U0RTSN	Ready to send	O	When hardware flow control is disabled, programming the UART_CTL0 bit 6 directly controls this output. That is, this pin is the inverse of the UART_CTL0 bit 6. Hardware flow control is disabled by default. If receive hardware flow control is enabled through writing the UART_CTL1 bit 7 to 1, ready to send signal will be auto generated in hardware. In this case, U0RTSN remains high as long as the number of unread bytes in the Rx FIFO is greater than the configured threshold value, which is specified in the UART_CTL1 bit 0 to bit 6.
U0CTSN	Clear to send	I	The value of this input signal is indicated by the UART_STS0 register bit 9 after logical inverse. When the U0CTSN input changes value, an interrupt is generated towards the MCU. If hardware flow control is enabled and the U0CTSN input pin is low, the UART immediately stops data transmission on the U0TXD output pin after it completes the current data byte transmission.
U0TRN	Data terminal ready	O	This output is directly controlled by programming the corresponding UART_CTL0 register bit 8. Please note that the output is the inverse of the register bit programmed.
U0DTSN	Data set ready	I	The value of this input signal is indicated by the UART_STS0 status register bit 8. When DSR input changes value, an interrupt is generated towards the MCU.

Note: If Ring Indication and Carrier Detect signals are required for this interface, they can be supplied by using two GPIO pins.

The size of Tx FIFO for the transmission is 128 bytes. It uses a FIFO pointer to monitor the number of data in the Tx FIFO that have not yet been transmitted. The MCU can read the UART_STS1 bits [15:8] to access the pointer.

The UART also uses a configurable Tx interrupt threshold that can be configured by writing to the UART_CTL2 register bits [14:8]. This field specifies the number of empty spaces that must be available in the Tx FIFO before issuing an interrupt. Whenever the number of empty spaces exceeds this value, an interrupt is generated to MCU (UART_STS0 Tx FIFO empty bit, bit 0). The interrupt bit in the UART_STS0 Tx FIFO empty bit is automatically cleared when the number of empty bytes in the Tx FIFO equals or falls below the specified Tx FIFO threshold.

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The size of Rx FIFO for receiving data is 128 bytes. It uses a pointer to monitor the number of characters in the Rx FIFO that have not yet been read by the MCU. The MCU can access the pointer by reading the UART_STS1 bits [7:0].

The UART also uses a configurable Rx interrupt threshold that can be configured by writing to the UART_CTL2 register bits [6:0]. This field specifies the number of unread data that must be available in the Rx FIFO before issuing an interrupt. Whenever the number of unread data exceeds this value, an interrupt is generated to the MCU. The interrupt is cleared by MCU reading the data out.

The UART interface also uses a receive timeout threshold, and the threshold can be configured by the UART_CTL1 bits [13:9]. Using the receive timeout interrupt prevents deadlocks, which occur when unread data are present in the Rx FIFO, but are not enough to generate a normal Rx interrupt. An Rx FIFO full interrupt (UART_STS0 bit 0) is always issued when the configured Rx timeout threshold time has elapsed and unread data are present in the Rx FIFO. When the CPU reads the last data in the Rx FIFO, the timer is reset and the interrupt is cleared automatically. Setting the timeout threshold to zero disables the timeout function.

When receiving data, UART also generate parity error/framing error if error condition appears. Also, if the receive FIFO over runs, an error interrupt is generated. Write to corresponding interrupt clear bits will clear these interrupts.

4.8.1.3 6-Wire UART Interface

This UART port is UART 0, used only by the MCU. It consists of the following pins.

- U0TXD, data output.
- U0RXD, data input.
- U0DTRN, active low.
- U0RTSN, active low.
- U0DSRN, active low.
- U0CTSN, active low.

The hardware flow control pins are also shared with JTAG pins, i.e., when JTAG is used, only Rx and Tx pins are available, reducing to a 2-wire UART port.

Similar to UART0, UART2 can also be used as either a 6-wire or a 2-wire interface. UART2 can be used by either the MCU or the DSP.

4.8.1.4 2-Wire UART Interface

This UART is UART 1 and can be used by either the MCU or DSP and consists of the following pins.

- U1TXD, data output.
- U1RXD, data input.

There is no hardware flow control for this UART interface.

4.8.1.5 UART Registers

MCU UART0 Base Address: 0x8300_0000
MCU UART1 Base Address: 0x8400_0000
MCU UART2 Base Address: 0x8E00_0000
DSP UART1 Base Address: 0xBE00
DSP UART2 Base Address: 0xBF00

Table 32: UART control registers.

DSP Address	MCU Address	Signal	Bit Pos	R/W	Default	Description
0xBE00	0x0000	UART_TXD	[7:0]	W only	N/A	Writing data to this address initiates a character transmission through Tx FIFO.
			[15:8]			Reserved.

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DSP Address	MCU Address	Signal	Bit Pos	R/W	Default	Description
0xBE01	0x0004	UART_RXD	[7:0]	R only	N/A	Reading this register retrieves the next data byte from the Rx FIFO.
			[15:8]			Reserved.
0xBE02	0x0008	UART_STS0	[15:0]	R only		
			[0]		0	Row Rx_fifo_full_tout. This bit is set when the number of Rx FIFO data bytes is larger than the Rx interrupt watermark value or when receive time is out. Auto cleared when the condition disappears.
			[1]		0	Row Tx_fifo_empty This bit is set when the number of Tx FIFO data bytes is less than the Tx interrupt watermark value. Auto cleared when the condition disappears.
			[2]		0	Row parity error
			[3]		0	Row framing error
			[4]		0	Row rxf_overrun
			[5]		0	Row dsr_change
			[6]		0	Row cts_change
			[7]		0	Row break_detect
			[8]		0	DSR: Data set ready
			[9]		0	CTS: clear to send
			[10]		0	RTS: Request to send
			[11]		0	RXD: Rx data in
			[12]		0	TXD: Tx data out
			[13]		0	Rx_tout: This bit is set when receive time is out. Auto cleared when the condition disappears.
			[15:14]			Reserved.
0xBE03	0x000C	UART_STS1	[7:0]		0	Rx_fifo_cnt
			[15:8]		0	Tx_fifo_cnt
0xBE04	0x0010	UART_IEN	[7:0]	R only		
			[0]		0	Rx_fifo_full interrupt enable
			[1]		0	Tx_fifo_empty interrupt enable
			[2]		0	Parity_error interrupt enable
			[3]		0	Framing_error interrupt enable
			[4]		0	Rxf_overrun interrupt enable
			[5]		0	Dsr_change interrupt enable
			[6]		0	Cts_change interrupt enable
			[7]		0	Break_detect interrupt enable
			[12:8]		0	Reserved.
			[13]		0	Rx_tout interrupt enable
			[15:8]		0	Reserved.
0xBE05	0x0014	UART_ICLR	[7:0]	W only		
			[0]		0	Reserved.
			[1]		0	Reserved.
			[2]		0	Write “1” clear parity_error interrupt
			[3]		0	Write “1” clear framing_error interrupt
			[4]		0	Write “1” clear rx_fifo_overrun interrupt

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DSP Address	MCU Address	Signal	Bit Pos	R/W	Default	Description
			[5]		0	Write “1” clear dsr_change interrupt
			[6]		0	Write “1” clear cts_change interrupt
			[7]		0	Write “1” clear break_detect interrupt
			[12:8]		0	Reserved.
			[13]		0	Write “1” clear Rx_tout interrupt
			[15:14]		0	Reserved.
0xBE06	0x0018	UART_CTL0	[8:0]			
		Odd_Parity	[0]		0	Odd parity. 0: even parity, 1: odd parity.
		Parity_enable	[1]		0	Parity enable. 0: parity disabled, 1: parity enabled.
		Byte_length	[3:2]		0x3	Data byte length. 0: 5 bits, 1: 6 bits, 2: 7 bits, 3: 8 bits.
			[5:4]		0x3	Stop bit number. 0: unused, 1: 1stop bit, 2: 1.5 stop bits, 3: 2 stop bits.
			[6]		0	Ready To Send When receive hardware flow control is not set, this bit controls the output of RTSN. When receive hardware flow is set, this bit is controlled by the Rx FIFO level.
			[7]		0	Send Break When Tx FIFO is empty and Tx is idle, setting this bit forces the Tx data output low. Need to be cleared by MCU.
			[8]		0	Data Terminal Ready This bit controls the DTRN output
		Ir_tx_iv	[9]		0	IrDA TX polarity inverse
		Ir_rx_iv	[10]		0	IrDA RX polarity inverse
		Ir_tx_en	[11]		0	IrDA TX enable
		Ir_dplx	[12]		0	IrDA TX/RX enable
		Ir_wctl	[13]		0	Set “1”, increase pulse width for one clock.
			[15:14]			Reserved.
0xBE07	0x001C	UART_CTL1	[13:0]			
			[6:0]		0	Receive Hardware Flow Control Threshold. When receive hardware flow control is enabled, if the number of unread bytes in the Rx FIFO is greater than the receive hardware flow control threshold value, the RTSN is set to high to stop the remote TX. RTS bit in the control register is also cleared at this time.

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DSP Address	MCU Address	Signal	Bit Pos	R/W	Default	Description
			[7]		0	Receive Hardware Flow Control Enable
			[8]		0	Transmit Hardware Flow Control Enable
			[13:9]		0	Receive Timeout Value
			[14]		0	UART self Loop: Tx input to RX
			[15]			Reserved.
0xBE08	0x0020	UART_CTL2	[14:0]			
			[6:0]		0	Receive Interrupt Watermark
			[7]			Reserved.
			[14:8]		0	Transmit Interrupt Watermark
			[15]			Reserved.
0xBE09	0x0024	UART_CKD0	[15:0]		0x054A	Clock divisor bit 0 to 15
0xBE0A	0x0028	UART_CKD1	[4:0]		0	Clock divisor bit 16 to 20
			[15:5]			Reserved.
0xBE0B	0x002C	UART_STS2	[15:0]	R only		Masked STS0 register, masked by IEN register.
			[0]		0	Masked Rx_fifo_full This bit is set when the number of Rx FIFO data bytes is larger than the Rx interrupt watermark value or when receive time is out. Auto cleared when the condition disappears.
			[1]		0	Masked Tx_fifo_empty This bit is set when the number of Tx FIFO data bytes is less than the Tx interrupt watermark value. Auto cleared when the condition disappears.
			[2]		0	Masked parity error
			[3]		0	Masked framing error
			[4]		0	Masked Rxf_overrun
			[5]		0	Masked Dsr_change
			[6]		0	Masked Cts_change
			[7]		0	Masked Break detect
			[12:8]		0	Reserved.
			[13]		0	Masked Rx_tout interrupt
			[15:14]		0	Reserved.

4.8.2 IrDA Interface

All the UART ports, UART0, UART1 and UART2, have a built-in IrDA controller. They can be configured to connect to an IrDA transceiver, resulting in one or two IrDA interfaces. When used as regular UART port, the IrDA controller is bypassed.

4.8.2.1 IrDA Controller

The IrDA controller controls the off-chip infrared transceiver to transmit and receive serial infrared data.

The modulation method of the transmitted data varies based on the data rates. Two classes of data rates are used in IrDA data exchange (2 slightly different modulation exists in the first class): Slow data rates ranging from 2.4 k bits/s to 115 k bits/s, and Fast data rates, ranging from 115.2 k bits/s to 4 M bits/s. The supporting of the different modulation methods is left to the software to implement and the IrDA controller in SC6600D provides the waveform generation circuits for the data transmission and the

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receive signal edge detection circuits for the data receiving. This implementation achieves better compatibility but the MCU loading for the IrDA control is bigger.

The IrDA data input and output pins are shared with the UART RXD and TXD pins, thus when IrDA is enabled, the corresponding UART will not be available.

The MCU can transmit data on the output lines through a pair of double-registered address, which are ir_tx_ppls_wdth and ir_rx_npls_wdth. By means of these special registers, the MCU can directly form the shape of an amplitude-modulated signal on the output line.

The MCU can form an output signal by continuously writing a pair of data to the double-buffered registers, which are the ir_tx_ppls_wdth and ir_rx_npls_wdth registers. These pairs consist of a sequence of square-wave pulse followed by a sequence of silence periods. The width of pulse and silent periods is specified by the value written to the ir_tx_ppls_wdth and ir_rx_npls_wdth registers. The unit of these values is the square wave modulation clock frequency. The square wave modulation signal is generated by pre-scale the MCU clock using the value programmed in the ir_tx_dvdr register. After each transmission, a pair of ir_tx_ppls_wdth and ir_rx_npls_wdth value is used up and an interrupt is send to the MCU. The default value of the square wave modulation clock frequency is 0x196.

When the ir_tx_ppls_wdth and ir_rx_npls_wdth value is used up and no new data are written to these registers, the transmit line is driven to LOW.

The IrDA controller sense the level changes on the receive line to receive the IrDA data. The MCU can indirectly read the shape of the received signal by means of level change notifications. Depending on the configured definition of a level change notification, the MCU is notified when a HIGH to LOW transition (or alternatively a LOW to HIGH transition, or alternatively on any type of transition) is detected on the input line. The duration between the last change and the current change is saved in the receive FIFO for MCU to read. The receive FIFO is 8 word long (16 bit in width).

The MCU decode the received data in software to determine the final data/commands received.

4.8.2.2 IrDA Control Registers

IrDA0 Base Address: 0x8300_0000
IrDA1 Base Address: 0x8400_0000
IrDA2 Base Address: 0x8e00_0000

Note:

- When IrDA0 is enabled, UART0 should not be used. When IrDA1 is enabled, UART1 should not be used. When IrDA2 is enabled, UART2 should not be used.
- Most IrDA control registers are shared with UART control register.

Table 33: IrDA control registers.

DSP Address	MCU Address	Signal	Bit Pos	R/W	Default	Description
0xBE00	0x0000	UART_TXD	[7:0]	W only	N/A	Writing data to this address initiates a character transmission through Tx FIFO.
			[15:8]			Reserved.
0xBE01	0x0004	UART_RXD	[7:0]	R only	N/A	Reading this register retrieves the next data byte from the Rx FIFO.
			[15:8]			Reserved.
0xBE02	0x0008	UART_STS0	[15:0]	R only		

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DSP Address	MCU Address	Signal	Bit Pos	R/W	Default	Description
			[0]		0	Row Rx_fifo_full_tout. This bit is set when the number of Rx FIFO data bytes is larger than the Rx interrupt watermark value or when receive time is out. Auto cleared when the condition disappears.
			[1]		0	Row Tx_fifo_empty This bit is set when the number of Tx FIFO data bytes is less than the Tx interrupt watermark value. Auto cleared when the condition disappears.
			[2]		0	Row parity error
			[3]		0	Row framing error
			[4]		0	Row rxf_overrun
			[5]		0	Row dsr_change
			[6]		0	Row cts_change
			[7]		0	Row break_detect
			[8]		0	DSR: Data set ready
			[9]		0	CTS: clear to send
			[10]		0	RTS: Request to send
			[11]		0	RXD: Rx data in
			[12]		0	TXD: Tx data out
			[13]		0	Rx_tout: This bit is set when receive time is out. Auto cleared when the condition disappears.
			[15:14]			Reserved.
0xBE03	0x000C	UART_STS1	[7:0]		0	Rx_fifo_cnt
			[15:8]		0	Tx_fifo_cnt
0xBE04	0x0010	UART_IEN	[7:0]	R only		
			[0]		0	Rx_fifo_full interrupt enable
			[1]		0	Tx_fifo_empty interrupt enable
			[2]		0	Parity_error interrupt enable
			[3]		0	Framing_error interrupt enable
			[4]		0	Rxf_overrun interrupt enable
			[5]		0	Dsr_change interrupt enable
			[6]		0	Cts_change interrupt enable
			[7]		0	Break_detect interrupt enable
			[12:8]		0	Reserved.
			[13]		0	Rx_tout interrupt enable
			[15:8]		0	Reserved.
0xBE05	0x0014	UART_ICLR	[7:0]	W only		
			[0]		0	Reserved.
			[1]		0	Reserved.
			[2]		0	Write “1” clear parity_error interrupt
			[3]		0	Write “1” clear framing_error interrupt
			[4]		0	Write “1” clear rx_fifo_overrun interrupt
			[5]		0	Write “1” clear dsr_change interrupt
			[6]		0	Write “1” clear cts_change interrupt

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DSP Address	MCU Address	Signal	Bit Pos	R/W	Default	Description
			[7]		0	Write “1” clear break_detect interrupt
			[12:8]		0	Reserved.
			[13]		0	Write “1” clear Rx_tout interrupt
			[15:14]		0	Reserved.
0xBE06	0x0018	UART_CTL0	[8:0]			
		Odd_Parity	[0]		0	Odd parity. 0: even parity, 1: odd parity.
		Parity_enable	[1]		0	Parity enable. 0: parity disabled, 1: parity enabled.
		Byte_length	[3:2]		0x3	Data byte length. 0: 5 bits, 1: 6 bits, 2: 7 bits, 3: 8 bits.
			[5:4]		0x3	Stop bit number. 0: unused, 1: 1stop bit, 2: 1.5 stop bits, 3: 2 stop bits.
			[6]		0	Ready To Send When receive hardware flow control is not set, this bit controls the output of RTSN. When receive hardware flow is set, this bit is controlled by the Rx FIFO level.
			[7]		0	Send Break When Tx FIFO is empty and Tx is idle, setting this bit forces the Tx data output low. Need to be cleared by MCU.
			[8]		0	Data Terminal Ready This bit controls the DTRN output
		Ir_tx_iv	[9]		0	IrDA TX polarity inverse
		Ir_rx_iv	[10]		0	IrDA RX polarity inverse
		Ir_tx_en	[11]		0	IrDA TX enable
		Ir_dplx	[12]		0	IrDA TX/RX enable
		Ir_wctl	[13]		0	Set “1”, increase pulse width for one clock.
			[15:14]			Reserved.
0xBE07	0x001C	UART_CTL1	[13:0]			
			[6:0]		0	Receive Hardware Flow Control Threshold. When receive hardware flow control is enabled, if the number of unread bytes in the Rx FIFO is greater than the receive hardware flow control threshold value, the RTSN is set to high to stop the remote TX. RTS bit in the control register is also cleared at this time.

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DSP Address	MCU Address	Signal	Bit Pos	R/W	Default	Description
			[7]		0	Receive Hardware Flow Control Enable
			[8]		0	Transmit Hardware Flow Control Enable
			[13:9]		0	Receive Timeout Value
			[14]		0	UART self Loop: Tx input to RX
			[15]			Reserved.
0xBE08	0x0020	UART_CTL2	[14:0]			
			[6:0]		0	Receive Interrupt Watermark
			[7]			Reserved.
			[14:8]		0	Transmit Interrupt Watermark
			[15]			Reserved.
0xBE09	0x0024	UART_CKD0	[15:0]		0x054A	Clock divisor bit 0 to 15
0xBE0A	0x0028	UART_CKD1	[4:0]		0	Clock divisor bit 16 to 20
			[15:5]			Reserved.
0xBE0B	0x002C	UART_STS2	[15:0]	R only		Masked STS0 register, masked by IEN register.
			[0]		0	Masked Rx_fifo_full This bit is set when the number of Rx FIFO data bytes is larger than the Rx interrupt watermark value or when receive time is out. Auto cleared when the condition disappears.
			[1]		0	Masked Tx_fifo_empty This bit is set when the number of Tx FIFO data bytes is less than the Tx interrupt watermark value. Auto cleared when the condition disappears.
			[2]		0	Masked parity error
			[3]		0	Masked framing error
			[4]		0	Masked Rxf_overrun
			[5]		0	Masked Dsr_change
			[6]		0	Masked Cts_change
			[7]		0	Masked Break detect
			[12:8]		0	Reserved.
			[13]		0	Masked Rx_tout interrupt
			[15:14]		0	Reserved.

4.8.3 SPI Interface

SC6600D provides up to 3 SPI interface ports, which share the pins with UART and IrDA.

Table 34: Organization of the serial ports.

	Serial port 0	Serial port 1	Serial port 2
User	MCU	Shared	Shared
Function 1	UART 0	UART 1	UART 2
Function 2	SPI 0	SPI 1	SPI 2
Function 3	IrDA 0	IrDA 1	IrDA 2

The signals are mapped to the pins as shown in the following table.

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Table 35: Pin mapping for the serial ports.

UART Pins	SPI Pins
UART_TXD	SPI_DO
UART_RXD	SPI_DI
UART_DTRN	SPI_CLK
UART_RTSN	SPI_CSN0
UART_DSRN	SPI_CSN1
UART_CTSN	SPI_CSN2
	SPI_CSN3

4.8.3.1 SPI Registers

MCU SPI0 Base Address: 0x8300_0000
MCU SPI1 Base Address: 0x8400_0000
MCU SPI2 Base Address: 0x8E00_0000
DSP SPI1 Base Address: 0xBE00
DSP SPI2 Base Address: 0xBF00

Table 36: SPI control registers (base address: 0x8300_0000, 0xBE00).

SPI1 DSP Address	SPI012 ARM Address	Signal	Bit Pos	R/W	Default	Description
0xBE00	0x0000	spi_txd	[31:0]	R/W	N/A	Write data to this address initiates a character transmission through Tx FIFO.
0xBE01	0x0004	spi_sts0	[15:0]	R only		
			[0]		0	Raw Rx_fifo_full_tout. This bit is set when the number of Rx FIFO data bytes is larger than the Rx interrupt watermark value or when receive time is out. Auto cleared when the condition disappears.
			[1]		0	Row Tx_fifo_empty This bit is set when the number of Tx FIFO data bytes is less than the Tx interrupt watermark value. Auto cleared when the condition disappears.
			[2]		0	Raw rxf_overrun
			[3]		0	Data bus busy
			[4]		0	RXD: Rx data in
			[5]		0	TXD: Tx data out
			[31:6]			Reserved.
0xBE02	0x0008	spi_sts1	[13:0]	R only		
			[5:0]		0	Rx_fifo_cnt
			[7:6]			
			[13:8]		0	Tx_fifo_cnt
			[31:14]			
0xBE03	0x000C	spi_ien	[7:0]	R/W		
			[0]		0	Rx_fifo_full_tout interrupt enable
			[1]		0	Tx_fifo_empty interrupt enable
			[2]		0	Rxf_overrun interrupt enable
			[31:3]			Reserved.

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SPI1 DSP Address	SPI012 ARM Address	Signal	Bit Pos	R/W	Default	Description
0xBE04	0x0010	spi_ctl0	[7:0]	R/W		
			[4:0]		0	Write “1” enables Rx data shift in at clock neg-edge
			[1]		0	Write “1” enables Tx data shift out at clock neg-edge
			[6:2]		0	Transmit data bit number, “1”: 1bit per word, “0”: 32 bit per word
			[3]		0	Write “1” enables data transmit/receive from LSB.
			[11:8]		0	Four bit chip select. There are totally 4 chip selects for SPI.
			[14:12]			Reserved.
			[15]	W only		“1” Receive data only. Write this bit separately after initialize other registers.
			[31:16]			Reserved.
0xBE05	0x0014	Spi_ctl1		R/W		
			[4:0]		0	Receive Data full threshold
			[9:5]		0	Transmit Data empty threshold
			[14:10]			Reserved.
			[15]		0	DMA_en
0xBE06	0x0018	Spi_ctl2	[15:0]	R/W	0	
			[4:0]		0	2-wire mode, w/r control bit position
			[5]		0	“1” enable 2-wire mode
			[6]		0	2-wire mode, read command polarity
			[7]		0	S8 mode (LCD S8)
			[9:8]		0	S8 cd maps to csn number
			[10]		0	2-wire Melody timing 2, csn high mode enable
			[11]		0	2-wire Melody timing 1, csn high mode enable
			[15:12]		0	Csn high bit enable, “0x0001” enable csn0 high.
0xBE07	0x001C	Spi_clkd	[15:0]		0x0003	Clock divisor bit 0 to 15
0xBE08	0x0020	Spi_sts2	[15:0]	R only		Masked STS0 register, masked by IEN reg.
			[0]		0	Masked Rx_fifo_full_tout. This bit is set when the number of Rx FIFO data bytes is larger than the Rx interrupt watermark value or when receive time is out. Auto cleared when the condition disappears.

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SPI1 DSP Address	SPI012 ARM Address	Signal	Bit Pos	R/W	Default	Description
			[1]		0	Masked Tx_fifo_empty This bit is set when the number of Tx FIFO data bytes is less than the Tx interrupt watermark value. Auto cleared when the condition disappears.
			[2]		0	Masked rxf_overrun
			[15:3]			Reserved.
0xBE09	0x0024	SPI_ICLR	[2:0]	W only		
			[0]		0	Reserved.
			[1]		0	Reserved.
			[2]		0	Write "1" clears Rx over run interrupt.
			[15:3]			Reserved.
0xBE0A	0x0028	SPI_ctl3	[15:0]			
			[7:0]		0	2-wire Melody, read start bit address
			[12:8]		0	Transmit data interval, programmable from 0 to 255 clock cycles.
			[13]		0	Reserved.
			[14]		0	Reserved.
			[15]		0	Reserved.

4.8.4 SIM Card Interface

The SIM card interface is implemented according to the GSM SIM card standard and supports T = 0 protocol only. The SIM card interface is to transfer data from/to a SIM card in an asynchronous fashion in half duplex mode through a bi-directional I/O pin.

The SIM interface consists of the following dedicated pins.

- SIMCLK, SIM clock.
- SIMDA, SIM data.
- SIMPE, SIM power enable.
- SIMRST, SIM reset.

4.8.4.1 SIM Functional Description

The Features for the SIM card controller in SC6600D include:

- Automatic activation and deactivation sequence.
- Programmable generation of clock to the SIM card.
- Programmable transmission baud rate.
- Support for T = 0 asynchronous protocol type.
- One 16 byte Tx FIFO and one 16 byte Rx FIFO.
- Parity checking and error handling.

The SIM interface module is designed to support different external SIM driver chips, including TDA8003 and LM1555. When using TDA8003, the activation and deactivation will be performed by TDA8003 and thus activation/deactivation in SC6600D should be disabled. When using LM1555, the activation and deactivation of the SIM card is fully controlled by SC6600D.

Please refer to TDA8003 and LM1555 datasheet and the SIM register document for further details.

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4.8.4.2 SIM Clock and Baud Rate Control

The SIM card clock is generated and sent from the SIM card controller to the SIM card. The SIM_CTL1 register bits [10:8] decide the generated SIM clock frequency.

Table 37: SIM clock control.

Clock mode, 0x8500_001C [10:8]	SIM clock frequency
0	MCU clock / 2
1	MCU clock / 4
2	MCU clock / 8
3	MCU clock / 16
4	MCU clock / 32
5	MCU clock / 64
6	MCU clock / 128
7	MCU clock / 256

The baud rate that the SIM card controller uses in Tx and Rx is controlled through programming SIM_CLK_DVD register.

The clock output to the SIM card needs to match the baud rate that the SIM card controller uses so that the Rx and Tx can be done correctly.

4.8.4.3 SIM Activation and Deactivation

For TDA8003, SC6600D controls its activation and deactivation functions by programming its command registers using the two-wire serial bus.

For LM1555, SC6600D controls the activation and deactivation process with the SIM control registers. The following are brief list of commands for the activation and deactivation functions.

- Program active_deactiva_en bit to 1 to enable the activation/deactivation function.
- Program do_act bit to 1 to start the activation sequence.
- (Program do_deact bit to 1 to start the deactivation sequence.)
- By programming the auto_active_deactive to 1, the activation will be executed when a card is inserted and the deactivation will be executed when the card is removed.

4.8.4.4 Activation and Deactivation

The SIM card controller is implemented with the following modules: SIM card activation/deactivation control, SIM card Rx/Tx control, Rx and Tx FIFO and related FIFO controls, SIM card I/O control, and SIM card control registers.

The activation/deactivation control module controls the activation/deactivation sequence of the SIM interface. After sending an activate command (writing 1 to SIM_CTL0 register bit 11) or a deactivate command (writing 1 to SIM_CTL0 register bit 12), the activation sequence or deactivation sequence will be sent to the SIM card. With the auto_active_deactive bit in SM_CTL0 register (bit 14) enabled, the activate/deactivate will be done automatically when card insertion/removal happens.

4.8.4.5 SIM Data Tx and Rx

The Tx will start when the tx_enable is 1. There is data in the FIFO and the last Rx is completed. The tx_int_mark sets the condition under which the tx_int will happen. When the empty entry in the tx_fifo is less than tx_int mark, tx_empty int will be set.

The Rx will start when the rx_enable is 1, when the last Tx is done and there is data coming in from the data input. The rx_int_mark sets the condition under which the rx_int will happen. When the data entry in the rx_fifo is greater than rx_int mark, rx_full int will be set.

The bit_convention decides the MSB and LSB in the Tx/Rx serial data, logic_level decides if the high electrical level represents the logic 1 in Tx/Rx serial data, and odd_parity bit decides if using odd or even parity in Tx/Rx data.

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In the SIM interface module, a timer is also designed to check if the receive portion is idle for a certain period of time and generate an interrupt when it happens. The watch_dog_count_limit defines the idle period in data bit streaming. Watch_dog_repeat_en decide if the timer start right after the interrupt is acknowledged (the interrupt is cleared). Write 1 to watch_dog_trigger start the timer counting. Any activity in the Rx portion will reset the timer counting.

4.8.4.6 Rx/Tx Control

The Rx/Tx control module controls the transmitting and receiving data to/from the SIM card. The SIM card controller receives/transmits data according to the data-level and bit-ordering that are specified in the Logic_level (bit 1) and Bit_convention (bit 0) bits in the SIM_CTL0 register. The data format is: 10 bits per character, 1 start bit + 8 data bits + 1 parity bit.

The SIM card controller includes a 16 byte Tx FIFO for data transmission. It uses a pointer to monitor the number of data in the Tx FIFO that have not yet been transmitted. The MCU can access the pointer by reading the SIM_STS1 register bit 4 to bit 0.

The SIM card controller also uses a configurable Tx interrupt threshold that can be configured by writing to the SIM_CTL1 register bit 4 to 7. This field specifies the number of empty characters that should be available in the Tx FIFO before issuing an interrupt. Whenever the number of empty characters exceeds this value, an interrupt is generated to the MCU. This interrupt is automatically cleared when the number of empty bytes in the Tx FIFO equals or falls below the specified Tx interrupt threshold value.

The SIM card controller also includes a 16 byte Rx FIFO for data receiving. It uses a pointer to monitor the number of bytes in the Rx FIFO that have not yet been read by the MCU. The MCU reads the SIM_STS1 register bit 0 to 4 to access the pointer.

The SIM card controller also uses a configurable Rx interrupt threshold. Which can be configured by writing to the SIM_CTL1 register bit 0 to 3. This field specifies the number of unread data that should be available in the Rx FIFO before issuing an interrupt. Whenever the number of unread data exceeds this value, an interrupt is generated to the MCU. This interrupt is automatically cleared when the number of unread data in the Rx FIFO equals or falls below the specified Rx interrupt threshold value.

4.8.4.7 Retransmission

The SIM card controller supports retransmission upon detecting an error condition. The SIM card controller checks the I/O line from the SIM card 11 bits after the start bits leading edge. If the detected I/O is a zero (error ACK), it assumes an error occurred and retransmits the byte. If the error ACK signal is repeated for the programmable number of times specified in the SIM_SHE register. The SIM card interface sets the bad Tx parity error bit in the status register (SIM_STS0 bit 3) and issues an interrupt.

For the transmission from the SIM card controller to the SIM card, when the SIM card controller detects a parity error following the transmission of a data byte, it performs the following sequence:

- The SIM card interface retransmits the data.
- If the retransmission succeeds, it ignores the initial failure.
- If the retransmission fails for the number of times specified in the programmable SIM_SHE register, the SIM card interface sets the bad parity bit interrupt the SIM_STS0 register, issues an interrupt to the MCU, and stops retransmission of the byte.

4.8.4.8 SIM Power Supply

The SIMPE output signal controls the power supply of the SIM card. During the activation/deactivation process, SIMPE output is automatically controlled. The assertion/desertion of SIMPE can also be controlled by directly programming the SIM_CTL0 register bit 7.

4.8.4.9 Unresponsive Card Detection

The SIM interface can detect an unresponsive card by means of a watchdog timer function, which determines the maximum allowable time that a data byte should take to arrive from the SIM card. The MCU can configure the watchdog timer by programming the SIM_WDT register. The watchdog timer can function in two modes: auto mode and single mode. In the auto mode, the watchdog timer is continuously enabled. In the single mode, the watchdog timer disables itself when a data byte is received from the card, or after it has timed out.

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4.8.4.10 SIM Interface Watchdog

SC6600D provides two separate watchdogs.

- One watchdog is used to report Rx idle for a preprogrammed time.
- The other watchdog is for time out when RX retransmission is on error.

4.8.4.11 SIM Interface Separate Timing Control

SC6600D provides separate control registers and counters for Rx and Tx. This provides more timing control flexibility.

4.8.4.12 SIM Card Interface Registers

Table 38: SIM card interface registers (base address: 0x8500_0000).

Address	Signal	Bit Pos	R/W	Default	Description
0x0000	SIM_TX	[7:0]	W only		Writing to this register will send data to Tx FIFO and then the data get transmitted.
0x0004	SIM_RX	[7:0]	R only		Read from this address retrieve data from Rx FIFO.
0x0008	SIM_STS0	[15:0]	R/W		
	Rx_fifo_full	[0]		0	Rx FIFO data number bigger than rx_int_mark
	Tx_fifo_empty	[1]		1	Tx FIFO data number bigger than tx_int_mark
	Rx parity error	[2]		0	Interrupt status bit for Rx parity error
	Tx parity error	[3]		0	Interrupt status bit for Tx parity error
	Rx_tout/Unresp_card	[4]		0	Interrupt status bit for rx time out or card unresponsive
	Card_in	[5]		0	Interrupt status bit for card inserted
	Card_out	[6]		0	Interrupt status bit for card removed
	Early answer to reset	[7]		0	Interrupt status bit for early answer to reset
	Active done	[8]		0	Interrupt status bit to show activation is done
	Rx_tout	[9]		0	Interrupt status bit to show Rx time out under idle state.
		[15:10]			Reserved.
0x000C	SIM_STS1	[15:0]	R only		
	Rx_fifo_count	[4:0]		0	Rx FIFO data count, bit4 used for debug only.
	Tx_fifo_count	[9:5]		0	Tx FIFO data count, bit9 used for debug only.
	Card_inserted	[10]		0	Reflect of card in input pin
	Sim_data	[11]		0	Reflect of SIM data I/O pin
	Sim_active_status	[12]		0	Activation status, 1: activated. 0: not activated.
	Active_on	[13]		0	Busy in activation process
	Deactive_on	[14]		0	Busy in deactivation process
		[15]			Reserved.
0x0010	SIM_IE	[15:0]	R/W		
	Rx_full_ie	[0]		0	Enable bit for Rx full interrupt
	Tx_empty_ie	[1]		0	Enable bit for Tx empty interrupt
	Rx_parity_err_ie	[2]		0	Enable bit for Rx parity error

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Address	Signal	Bit Pos	R/W	Default	Description
	Tx_parity_err_ie	[3]		0	Enable bit for Tx parity error
	Unresp_card_ie	[4]		0	Enable bit for unresponsive card
	Card_in_ie	[5]		0	Enable bit for card-in
	Card_out_ie	[6]		0	Enable bit for card-out
	Early_atr_ie	[7]		0	Enable bit for early answer to reset
	Active_done_ie	[8]		0	Enable bit for active done
	Rx_tout_ie	[9]		0	Enable bit for rx time out
		[15:10]			Reserved.
0x0014	SIM_ICLR	[15:0]	W only		
	Rx_full_iclr	[0]		0	Interrupt clear bit for rx full int
	Tx_empty_iclr	[1]		0	Interrupt clear bit for tx empty int
	Rx_parity_err_iclr	[2]		0	Interrupt clear bit for rx_parity_error
	Tx_parity_err_iclr	[3]		0	Interrupt clear bit for tx_parity_error
	Unresp_card_iclr	[4]		0	Interrupt clear bit for unresp_card
	Card_in_iclr	[5]		0	Interrupt clear bit for card_in
	Card_out_iclr	[6]		0	Interrupt clear bit for card_out
	Early_atr_iclr	[7]		0	Interrupt clear bit for early answer to reset
	Active_done_iclr	[8]		0	Interrupt clear bit for active done
	Rx_tout_iclr	[9]		0	Interrupt clear bit for Rx time out
		[15:10]			Reserved.
0x0018	SIM_CTL0	[15:0]	R/W		
	Bit_convention	[0]		0	Bit convention: 0: MSB (bit 7) transmitted first 1: LSB (bit 0) transmitted first
	Logic_level	[1]		0	0: high logic level represent “0” 1: high logic level represent “1”
	Odd_parity	[2]		0	0: Even Parity 1: Odd Parity
	Loopback_mode	[3]		0	Transmit data looped back to receive.
	Rx_fifo_Reset	[4]		0	Reset the Rx FIFO
	Tx_fifo_reset	[5]		0	Reset the Tx FIFO
	Sim_reset	[6]		0	Reset the SIM card module
	Power_enable	[7]		0	Enable the Power supply to SIM card
	Card_out_latched	[8]		0	This bit will be 1 if card out happened.
	Rx_enable	[9]		0	Enable the SIM Rx
	Tx_enable	[10]		0	Enable the SIM Tx
	do_act	[11]		0	
	do_deact	[12]		0	
	Active_deactive_en	[13]		0	Enable the activation/deactivation procedure
	Auto_active_deactive	[14]		0	Enable the auto start of activation/deactivation when card-in or card-out happens.
	Tx_data_out_low	[15]		0	Force the Tx data to low logic level.
0x001C	SIM_CTL1	[15:0]	R/W		
	Rx_int_mark	[3:0]		0	Receive Interrupt Watermark
	Tx_int_mark	[7:4]		0	Transmit Interrupt Watermark

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Address	Signal	Bit Pos	R/W	Default	Description
	Clock_mode	[10:8]		0	Select the SIM clock speed. The SIM clock is divided from the arm bus clock: 0: MCU CLK/2 1: MCU CLK/4 2: MCU CLK/8 3: MCU CLK/16 4: MCU CLK/32 5: MCU CLK/64 6: MCU CLK/128 7: MCU CLK/256
	Clock_enable	[11]		0	Enable for the SIM clock output
	Clock_polarity	[12]		0	Set the polarity of the sim_clk signal when the SIM clock is stopped.
	Ad_speed_ctl	[15:13]		0	Control the speed of the active/deactive sequence. 0: slowest, 7: fastest.
0x0020	SIM_RX_CK_dvd	[15:0]	R/W	0x5952	SIM Rx clock divisor bit 0 to 15
0x0024	SIM_SHE	[15:0]			
	Rx_retrx_lmt	[3:0]		0	Rx retransmit limit
	Tx_retrx_lmt	[7:4]		0	Tx retransmit limit
		[12:8]			Reserved.
	Tx_etu_sel	[15:13]		0	Select the Tx etu divisor: 0x111: the Tx etu is decided by sim_tx_clock_divisor at address 0x0034 Others: the Tx etu is the same as Rx etu.
0x0028	SIM_TGC	[15:0]	R/W		
	Guard_time	[7:0]		0x30	Times in bit unit between the consecutive byte during data transmission to the SIM card.
	Turnaround_guard_time	[15:8]		0x30	Times in bit unit between the Rx and Tx.
0x002C	SIM_WDT	[15:0]	R/W		
	Watch_dog_rx_tout_en	[0]		0	Enable the Rx time out watch dog
	Watch_dog_rtx_tout_en	[1]		1	Enable the Rx retransmit watch dog timer. This timer watches when Rx retransmission is happening and it will flag the unresponsive card interrupt when the data from the SIM card is timed out (no data comes back).
	Watch_dog_count_limit	[15:2]		0x200	Watch dog timer limit for Rx retransmit watch dog
0x0030	SIM_INT_M	[15:0]	R/W		
	Rx_full_masked	[0]		0	Masked int bit for rx full int
	Tx_empty_masked	[1]		0	Masked int bit for tx empty int
	Rx_parity_err_masked	[2]		0	Masked int bit for rx_parity_error
	Tx_parity_err_masked	[3]		0	Masked int bit for tx_parity_error
	Unresp_card_masked	[4]		0	Masked int bit for unresp_card
	Card_in_masked	[5]		0	Masked int bit for card_in
	Card_out_masked	[6]		0	Masked int bit for card_out
	Early_atr_masked	[7]		0	Masked int bit for early answer to reset

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Address	Signal	Bit Pos	R/W	Default	Description
	Active_done_masked	[8]		0	Masked int bit for active done
		[15:8]			Reserved.
0x0034	SIM_TX_CK_dvd	[15:0]	R/W	0x5952	
	Sim_tx_clock_divisor				Clock divisor bit 0 to 15 for Tx data
0x0038	SIM_WDT1	[13:0]	R/W	0x0200	
	Watch_dog_count_limit1				Watch dog count limit for Rx time out.

4.8.5 Two-Wire Serial Interface

This serial port is on the MCU side and consists of the following pins.

- SDA, data.
- SCL, clock.

These two pins are also shared with a 3-wire serial port.

4.8.5.1 Features

The two-wire serial interface on SC6600D is a two-wire, bi-directional serial bus that provides a simple and efficient method of data exchange between devices. It is most suitable for applications requiring occasional communication over a short distance between many devices.

In general the two-wire interface defines 3 transmission speeds:

- Normal: 100 kbps
- Fast: 400 kbps
- High speed: 3.5 Mbps

Only normal and fast modes are supported on SC6600D. Another limitation is that only single master operations are supported on SC6600D.

The main features include the following.

- Software programmable clock frequency
- Software programmable acknowledge bit
- Interrupt driven data-transfers
- Start/Stop/Repeated Start/Acknowledge generation
- Supports Clock Stretching/Wait state generation
- Single Master Operation
- 8 word buffer mode support

4.8.5.2 Two-Wire Interface Connection

The two-wire serial interface uses a serial data line (SDA) and a serial clock line (SCL) for data transfers. All devices connected to these two signals must have open drain or open collector outputs. Both lines must be pulled-up to VCC by resistors. To reduce the number of system components, SC6600D provides the pull-up resistors on-chip.

4.8.5.3 Clock Divisor 0 & 1 Registers

This register is used to scale the SCL clock line. Due to the structure of the two-wire serial interface, the controller uses a 4*SCL clock signal internally. The clock divisor register must be programmed to this 4*SCL bit rate. Change the value of the clock register only when the ‘2ws_en’ bit is cleared. Otherwise, the register change will be ignored. 2ws_dvdr0 is the lower 16 bits of the divisor and 2ws_dvdr1 is the higher 10 bit (bit 0 ~ bit 9 map to clock divisor bit 16 ~ bit 25).

Example: CLK_I = 32 MHz, and the desired SCL = 100 KHz.

$$\text{Prescale} = \frac{32\,\text{MHz}}{4 \times 100\,\text{kHz}} = 80 = 0\text{x}50$$

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Therefore, the reset value is 0x50.

4.8.5.4 Operation

4.8.5.4.1 System Configuration

The two-wire serial system uses a serial data line (SDA) and a serial clock line (SCL) for data transfers. All devices connected to these two signals must have open drain or open collector outputs. The logic AND function is exercised on both lines with external pull-up resistors.

The two-wire serial controller implemented here is a single master device; therefore it starts generating a clock as soon as it is enabled. The user should program the clock to the desired value before starting any transfers.

Data is transmitted synchronously to SCL on the SDA line on a byte-by-byte basis. Each data byte is 8 bits long. There is one SCL clock pulse for each data bit with the MSB being transmitted first. There is an acknowledge bit following each transferred byte. Each bit is sampled during the high period of SCL; therefore the SDA line may be changed only during the low period of SCL and must be held stable during the high period of SCL. A transition on the SDA line while SCL is high is interpreted as a command (START or STOP command).

4.8.5.4.2 Two-wire Serial Protocol

Normally, a standard communication consists of four parts:

1. START signal generation
2. Slave address transfer
3. Data transfer
4. STOP signal generation

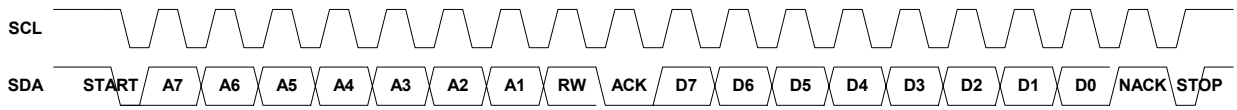

Figure 10: Two-wire serial interface protocol.

4.8.5.4.3 START signal

When the bus is free/idle, that is no master device is engaging the bus (both SCL and SDA lines are high), a master can initiate a transfer by sending a START signal. A START signal is defined as a high-to-low transition of SDA while SCL is high. The START signal denotes the beginning of a new data transfer.
A repeated START is a START signal without first generating a STOP signal. The master uses this method to communicate with another slave or the same slave in a different transfer direction (e.g. writing to device to reading from device) without releasing the bus.

The controller generates a START signal when the start bit in the 2ws_command Register (0x86000004) is set and the read or write bit is set. Depending on the current status of the SCL line a START or Repeated START is generated.

4.8.5.4.4 Slave Address Transfer

The first byte of data transferred by the master immediately after the START signal is the slave address. This is a seven-bit calling address followed by a RW bit. The RW bit signals the slave data transfer direction. No two slaves in the system can have the same address. Only the slave with an address that matches the one transmitted by the master will respond by returning an acknowledge bit by pulling the SDA low at the 9th SCL clock cycle.

The controller treats a Slave Address Transfer as any other write action. Store the slave device's address in the 2ws_command register and set the write bit. The controller will then transfer the slave address on the bus.

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4.8.5.4.5 Data Transfer

Once successful slave addressing is achieved, the data transfer can proceed on a byte-by-byte basis in the direction specified by the RW bit sent by the master. Each transferred byte is followed by an acknowledge bit on the 9th SCL clock cycle. If the slave signals a No Acknowledge (NACK), the master can generate a STOP signal to abort the data transfer or generate a repeated START signal and start a new transfer cycle.

If the master, as the receiving device, does not acknowledge the slave, the slave releases the SDA line for the master to generate a STOP or repeated START signal.

For writing data to a slave, store the data to transmit in the 2ws_command register and set the write bit. For reading data from a slave, set the read bit. When the transfer is done, an interrupt is generated to the MCU. The 2ws_command bits 8 to 15 contain valid data. The user may issue a new write or read command at this time.

4.8.5.4.6 STOP signal

The master can terminate the communication by generating a STOP signal. A STOP signal is defined as a low-to-high transition of SDA while SCL is at logical ‘1’.

4.8.5.5 Arbitration Procedure

Since the two-wire serial controller supports single master configurations only, no Arbitration logic is added to the controller. Only clock synchronization is supported since slave devices can use this mechanism for clock stretching.

4.8.5.5.1 Clock Synchronization

Since the logical AND function is performed on the signals, a high to low transition on SCL or SDA affect all devices connected to the bus. The SCL clock signal can be synchronized between multiple masters using this feature. Each device starts counting its SCL low period when the current master drives SCL low. Once a device’s clock has gone low, it holds the SCL line low until the clock high state is reached.

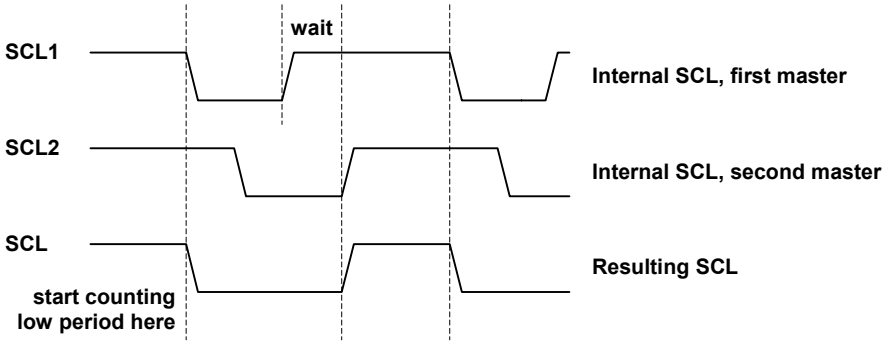

Figure 11: Clock synchronization on the two-wire serial bus.

4.8.5.5.2 Clock Stretching

Slave devices can use the clock synchronization mechanism to slow down the transfer bit rate. After the master has driven SCL low the slave can drive SCL low for the required period and then release it. If the slave’s SCL low period is greater than the master’s SCL low period, the resulting SCL bus signal low period is stretched, thus inserting wait-states.

4.8.5.6 Programming Examples

4.8.5.6.1 Example 1

Write 1 byte of data to a slave.

Slave address = 0x51 (b”1010001”)
Data to write = 0xAC

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Two-wire Serial Sequence:
1) Generate start command
2) Write slave address + write bit
3) Receive acknowledge from slave
4) Write data
5) Receive acknowledge from slave
6) Generate stop command

Commands:
1) Write 0xA225 to 0x86000004 (address + start bit + write cmd + iclr bit).
-- Wait for interrupt --
2) Read 2ws_ack bit from 0x86000004, should be ‘0’.
Write 0xAC15 to 0x86000004 (data + stop bit + write cmd + iclr bit)
-- Wait for interrupt --
3) Read 2ws_ack bit from 0x86000004, should be ‘0’.

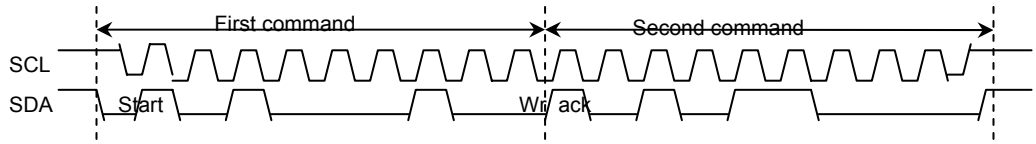

Figure 12: Two-wire serial port write example.

4.8.5.6.2 Example 2

Read a byte of data from a peripheral memory device.

Slave address = 100_1110
Memory location to read from = 0x20

Two-wire Serial sequence:
1) Generate start signal
2) Write slave address + write bit
3) Receive acknowledge from slave
4) Write memory location
5) Receive acknowledge from slave
6) Generate repeated start signal
7) Write slave address + read bit
8) Receive acknowledge from slave
9) Read byte from slave
10) Write no acknowledge (NACK) to slave, indicating end of transfer
11) Generate stop signal

Commands:
1) Write 0x9C25 to 0x86000004 (slave address (W bit) + start bit + write bit + iclr bit).
-- Wait for interrupt --
2) Read 2ws_ack bit from 0x86000004, should be ‘0’.
Write 0x2005 to 0x86000004 (memoery address + write bit + iclr bit).
-- Wait for interrupt --
3) Read 2ws_ack bit from 0x86000004, should be ‘0’.
Write 0x9D25 to 0x86000004 (slave address(R bit) + start bit + write bit + iclr bit).
-- Wait for interrupt --
4) Write 0x001B to 0x86000004 (stop bit + read bit + tx_ack + iclr bit).
5) Read 0x86000004 to get the read data D7 to D0;

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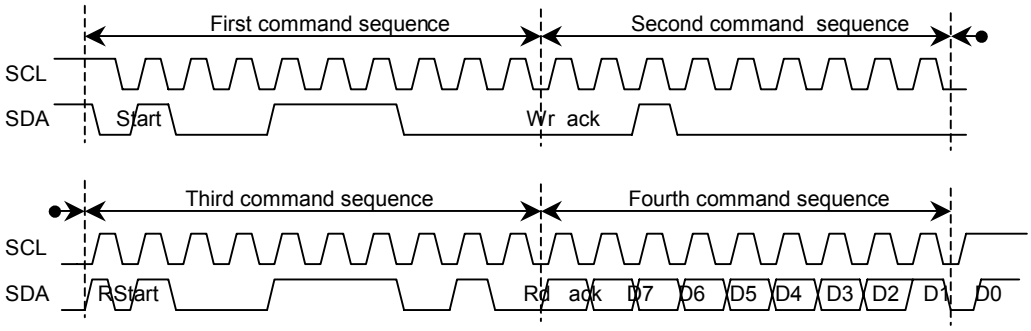

Figure 13: Two-wire serial port read example.

4.8.5.7 Two-Wire Serial Port Control Registers

Table 39: Two-wire serial port control registers (base address: 0x8600_0000).

Address	Signal	Bit Pos	R/W	Default	Description
0x0000	2ws_control	[15:0]	R/W		
	2ws_int	[0]		0	2ws interrupt
	2ws_ack	[1]		0	2ws received ack value
	2ws_busy	[2]		0	2ws data line value
	2ws_ie	[3]		0	2ws interrupt enable
	2ws_en	[4]		0	2ws module enable
	2ws_cmdbuf_en	[5]		0	Enable the command buffer mode
	2ws_cmd_exec	[6]		0	Start to exec the command in the command buffer
	2ws_st_cmdbuf	[9:7]		0	The state of 2ws command buffer state machine.
	2ws_cmdbuf_wptr	[12:10]		0	2ws command buffer write pointer
	2ws_cmdbuf_rptr	[15:13]			2ws command buffer read pointer
0x0004	2ws_command	[15:0]	R/W		
	Int_ack	[0]		0	2ws interrupt clear bit
	Tx_ack	[1]		0	2ws transmit ack that need to be send
	Cmd_write	[2]		0	2ws write command
	Cmd_read	[3]		0	2ws read command
	Cmd_stop	[4]		0	2ws stop command
	Cmd_start	[5]		0	2ws start command
	2ws_ack	[6]		0	2ws received ack value
	2ws_busy	[7]		0	2ws busy in exec commands
	2ws_data	[15:8]		0	2ws data received or data need to be transmitted
0x0008	2ws_divisor0	[15:0]	R/W	0x40	2ws clock divisor [15:0], default is 0x40.
0x000C	2ws_divisor1	[15:0]	R/W	0	2ws clock divisor [25:16], default is 0x0.
0x0010	2ws_rst	[15:0]	R/W		Write with bit 0 set to 1 will reset the 2ws module.
0x0014	2ws_cmd_buf	[15:0]	R/W		Write command to this register will save the command to the command buffer. Read from this register after the commands are all finished will return the results of the corresponding commands. The format of the command and the return result is the same as 2ws_command register.

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4.8.6 Keypad Interface

SC6600D provides a keypad interface that supports up to a keypad array of 6 x 5, or 30 keys and it consists of the following pins.

- KEYOUT [5:0], 6 row outputs.
- KEYIN [4:0], 5 column inputs.

No external pull-up resistors are needed when the internal pull-up at the input pads are enabled, see Figure 14.

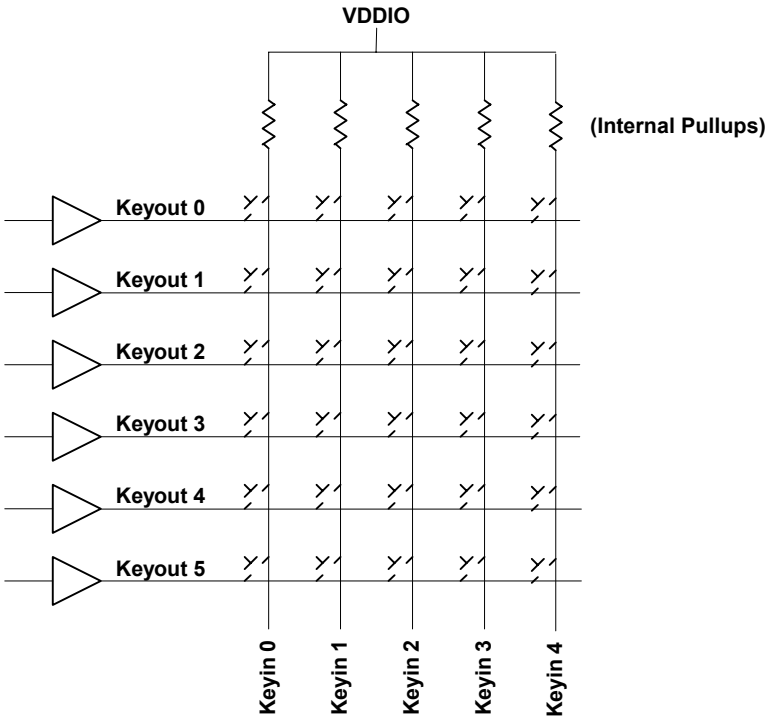

Figure 14: Keypad connection.

The keypad controller find the key pressed by periodically scan through the key matrix. Programming the control register, which is clk_divisor and clk_divisor1, controls the scan speed.

The keypad control logic provides two modes of operation, non-time-out mode and time-out mode.

4.8.6.1 Non-Time-Out Mode

In this mode, the keypad scan circuit will periodically scan through all the keys and if a key is pressed, the scan circuit will stay at this key until the key is released or the keypad interrupt is cleared. After that, it will scan the next key.

4.8.6.2 Time-Out Mode

In this mode, the keypad scan circuit will periodically scan through all the keys and if a key is pressed, the scan circuit will stay at this key for a preset period of time or until the keypad interrupt is cleared and then continue to scan the next key.

Thus, in Time-Out Mode, the software can detect 2 keys pressed at the same time while in Non-Time-Out Mode only one key press can be detected unless the software can clear the interrupt fast enough.

If a key is pressed, and the interrupt is cleared, the interrupt will be set again when the scan circuit goes back to that key. It does need more than 1 interrupt to check the key release.

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The mode select bit is at register at 0x8700_0004 bit 1, and the time period before scan to the next key is set by register at 0x8700_0014, bits 15:6. The time unit is base on the scan speed while the scan speed is defined by register at 0x8700_0010 bits 15:0, and 0x8700_0014 bit 5:0.

4.8.6.3 Sleep Mode

During sleep, all keypad inputs are OR'ed together to generate a wakeup trigger whenever a key is pressed.

4.8.6.4 Keypad Registers

Table 40: Keypad control registers (base address: 0x8700_0000).

Address	Signal	Bit Pos	R/W	Default	Description
0x0000	Keypad_sts	[15:0]	R only		
	Keypad_int	[0]			Keypad interrupt
	Time_out	[1]			Time out interrupt
	Row_count	[4:2]			Row counter
	Column_count	[7:5]			Column counter
		[8]			Key value
	Unused	[15:9]			
0x0004	Keypad_ctl	[15:0]	R/W		
	Keypad_ie	[0]		0	Keypad interrupt enable
	Keypad_timeout	[1]		0	Keypad timeout interrupt enable
	Keypad_enable	[2]		0	Keypad enable
	Read_iclr_en	[3]		0	When this bit is 1, keypad interrupt will be cleared by read the keypad status register.
	Row4_en	[4]		0	Enable bit for row 4
	Row5_en	[5]		0	Enable bit for row 5
	Row6_en	[6]		0	Enable bit for row 6
	Row7_en	[7]		0	Enable bit for row 7
	Col3_en	[8]		0	Enable bit for column 3
	Col4_en	[9]		0	Enable bit for column 4
	Spk_en	[10]		1	Speaker Interrupt enable
	Unused	[11]			Reserved
	Key_detect_time	[15:12]		0	Key in detection delay time.
0x0008	Keypad_iclr	[15:0]	W only		
	Keypad_int_iclr	[0]		0	Write 1 to this bit will clear the keypad int status bit.
	Keypad_toint_iclr	[1]		0	Write 1 to this bit will clear the keypad tout interrupt status bit.
		[2]			Reserved
	Pbint_iclr	[3]		0	Write 1 to this bit will clear the PBINT status bit.
	Unused	[8:4]			Reserved
	Spk_int_iclr	[9]		0	Write 1 to this bit will clear the speaker interrupt status bit
	Unused	[15:10]			
0x000C	Keypad_polarity	[12:8]	R/W		
	Row_polarity	[0:7]		0xFF	Internal row output XOR with this value to generate row output. This register is used to control the row output polarity.
	Column_polarity	[12:8]		0x1F	Column input XOR with this value to generate the interrupt column input. This register is used to control the column input polarity.
		[15:13]			Reserved
0x0010	Clk_divisor	[15:0]	R/W		

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Address	Signal	Bit Pos	R/W	Default	Description
	Clk_divisor	[15:0]		0	Clock divisor [15:0]
0x0014	Clk_divisor1	[15:0]	R/W		
		[5:0]		0	Reserved
	Tcnt_reg	[15:6]		0	Time out counter value
0x0018	Masked_int	[15:0]	R only		
	Masked_kpd_int	[0]		0	Keypad interrupt masked by the interrupt enable bit.
	Masked_tout_int	[1]		0	Keypad timeout interrupt masked by the time out interrupt enable bit.
	Charger_int	[2]		0	This bit reflects the charger_int input value. Charger interrupt comes from analog circuit.
	pbutton_int	[3]		0	This bit reflects the pbutton_int input value. Please note the pbutton_int input share the pin with the zbus address 3. Chip pin control register sel_reg5 [7:6] need to be 0 to select charger_int. It is selected by default.
		[8:4]		0	Reserved
	Spk_int	[9]		0	Speaker interrupt masked by speaker interrupt enable bit.
0x0028	Pbint_ctl	[31:0]	R/W		
	Pbint detect time	[3:0]			PBINT key detect time. If pbint_cnt_en bit is high, PBINT has to keep high for a period before it generates the interrupt to the MCU. The detection time is this register value multiplied by the RTC clock cycle. An interrupt will be generated after the detection time has passed, the interrupt status will be latched at PBINT status bit, and the MCU is able to clear it through pbint_iclr at keypad_iclr register bit [3].
		[27:4]			
	Pbint_status	[28]		0	PBINT latched status
	Pbint_hold_en	[29]			
	Pbint_detect_en	[30]		0	This bit high enable PBINT delay by the detect time.
	Pbint_cnt_en	[31]		0	If this bit is “0”, PBINT raw status will pass to interrupt controller without latch, the raw status shows in pbutton_int at address 0x0018. When this bit high, PBINT rising edge will be latched, the latched status shows at pbint_status bit.
0x002C	Pbing_cnt	[3:0]	R only		PBINT counter value
0x0030	Pbing_cnt_reg	[3:0]	R only		PBINT latched counter value

4.8.7 Pulse Width Modulation Outputs

SC6600D provides two PWM outputs that can be used to control a ringer or buzzer.

SC6600D generates the two PWM output signals from the MCU side, PWM_A and PWM_B. PWM_A is the combination of two identical but separately programmable PWM circuits, PWM0 and PWM1. The outputs from the two circuits are toggled at a rate of the PWM0 pre-scaled clock rate. By only enable the PWM0 or PWM1, the PWM_A can also be the PWM0 or PWM1 output. PWM_B is the output directly from the PWM3. Figure 15 shows the organization of PWM module.

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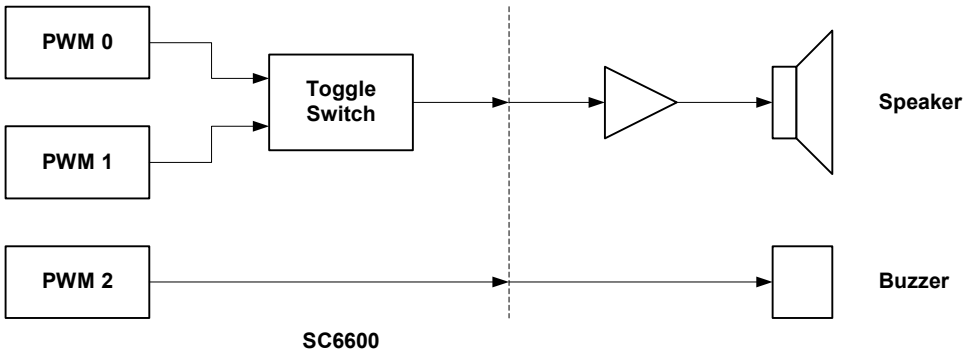

Figure 15: PWM module block diagram.

The operation of each of the PWM circuits is as described below.

The PWM uses the MCU peripheral bus clock to generate two pulse trains:

- A low frequency pulse train programmable to around 200 – 500 Hz. This is the Tone signal.
- A high frequency pulse train around 40 kHz with a variable duty cycle. This is the Mod signal.

The two pulse trains are mixed to produce the PWM output. The frequency of this output is the frequency of the Tone; the volume is dependent on the duty cycle of the Mod. The frequency of the Tone and the duty cycle of the Mod are programmable so that complex tones can be generated.

A PWM functional block diagram is shown in Figure 16.

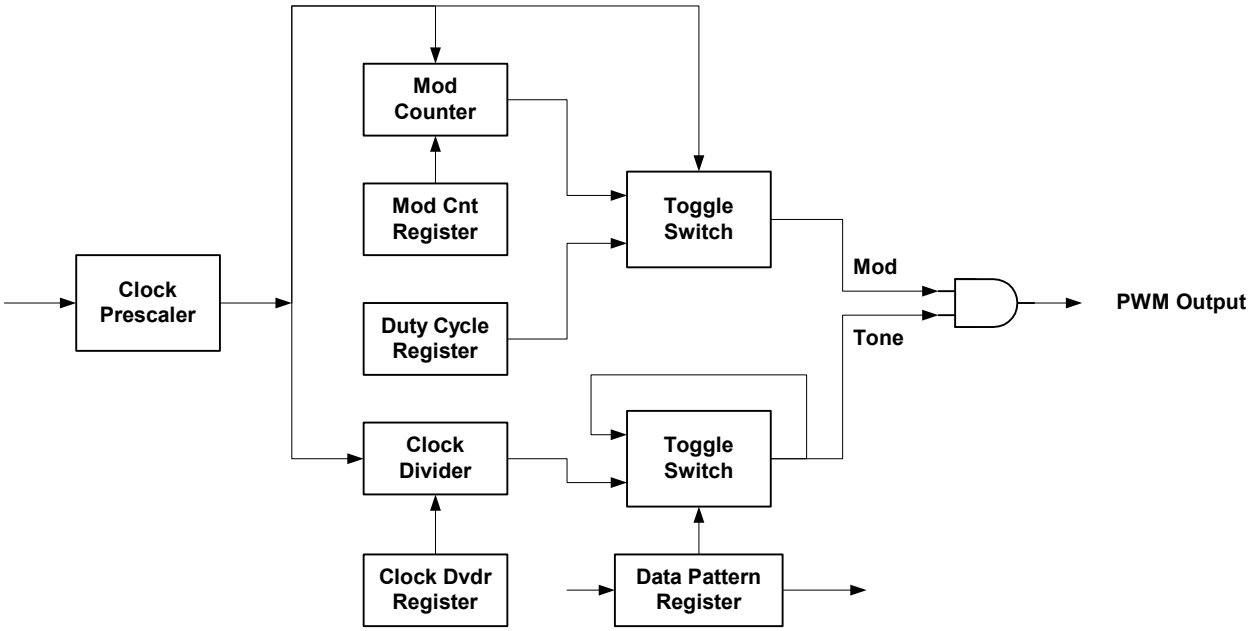

Figure 16: PWM module functional block diagram.

The Mod counter circuit is an 8-bit counter that is clocked around 4 MHz, which is the frequency of pre-scaled clock. The counter counts to the value set in the counter register and is then reset to 0. The default value of the counter register is decimal 100. The duty cycle register is a programmable 8-bit register. The duty cycle for the Mod is written to this register. The comparator function compares the counter output with the value of the duty cycle register. The output from the comparator is determined by the following rule:

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If Counter Value <= Duty Cycle Register, Comparator Output = 1, else Comparator output = 0.

The output from the comparator is the Mod signal. The duty cycle of the Mod signal is programmable by writing to the duty cycle register and to the Mod counter register. If the Mod counter register default value is used (decimal 100) the frequency of the Mod signal is pre-scaled clock /100.

The Clock Divisor Register is a programmable, 10-bit register. The divider circuit divides down the pre-scaled clock input by the value of the register to yield an output signal. The output from the divider is used to clock the Data Pattern Shift Register.

The Data Pattern Shift Register is a 32-bit serial shift register. The contents of the programmable Data Pattern Latch register are downloaded to the Data Pattern Shift Register to set the initial value of the shift register.

The output from the shift register is the time pulse train, Tone. This output is also fed back to the register input so that the same series of 32 bits are continuously cycled through the register. The data pattern is cycled at a frequency of (pre-scaled clock)/(clock divisor)/32.

The Mod and Tone pulse trains are ANDed to generate the output from the PWM circuit.

4.8.7.1 PWM Registers

Table 41: PWM control registers (base address: 0x8800_0000).

Address	Signal	Bit Pos	R/W	Default	Description
0x0000	Pwm0_prescale	[15:0]	R/W		
	Clk_prescaler	[7:0]			PWM 0 Clock prescaler
	Pwm_en0	[8]			PWM 0 enable
0x0004	Pwm0_cnt	[15:0]	R/W		
	Cnt_reg0	[7:0]			PWM 0 mod counter
	Duty_reg0	[15:8]			PWM 0 mod duty cycle
0x0008	Pwm0_dvd	[15:0]	R/W	0	PWM 0 tone divisor
0x000C	Pattern_reg0_15_0	[15:0]	R/W	0	PWM 0 pattern register low bits
0x0010	Pattern_reg0_31_16	[15:0]	R/W	0	PWM 0 pattern register high bits
0x0014	Pwm1_prescale	[15:0]	R/W		
	Clk_prescaler	[7:0]			PWM 1 Clock prescaler
	Pwm_en1	[8]			PWM 1 enable
0x0018	Pwm1_cnt	[15:0]	R/W		
	Cnt_reg1	[7:0]			PWM 1 mod counter
	Duty_reg1	[15:8]			PWM 1 mod duty cycle
0x001C	Pwm1_dvd	[15:0]	R/W	0	PWM 1 tone divisor
0x0020	Pattern_reg1_15_0	[15:0]	R/W	0	PWM 1 pattern register low bits
0x0024	Pattern_reg1_31_16	[15:0]	R/W	0	PWM 1 pattern register high bits
0x0028	Pwm2_prescale	[15:0]	R/W		
	Clk_prescaler	[7:0]			PWM 2 Clock prescaler
	Pwm_en2	[8]			PWM 2 enable
0x002C	Pwm2_cnt	[15:0]	R/W		
	Cnt_reg2	[7:0]			PWM 2 mod counter
	Duty_reg2	[15:8]			PWM 2 mod duty cycle
0x0030	Pwm2_dvd	[15:0]	R/W	0	PWM 2 tone divisor
0x0034	Pattern_reg2_15_0	[15:0]	R/W	0	PWM 2 pattern register low bits
0x0038	Pattern_reg2_31_16	[15:0]	R/W	0	PWM 2 pattern register high bits

Please note:

- There are 3 PWM modules. Only 2 outputs are going out of the chip. The first output is a combination of PWM0 and/or PWM1. The second output is from PWM2.

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4.8.8 MCU GPIO

SC6600D provides up to 59 GPIO pins from the MCU side, GPIO [58:0]. However, many of the pins are multiplexed with other functions and system design trade-off must be exercised on selecting them.

All the GPIO pins can be programmed to be either input or output. When in input mode, they can be programmed to trigger interrupt to the MCU.

4.8.8.1 MCU GPIO Control Registers

GPIO pin15~00 Register Base Address: 0x8A00_0000
GPIO pin31~16 Register Base Address: 0x8A00_0080
GPIO pin47~32 Register Base Address: 0x8A00_0100
GPIO pin58~48 Register Base Address: 0x8A00_0180

Charger-interrupt GPIO (input only) register base address: 0x8A00_0180 bit 2 (GPIO50)
Analog GPIO (input only) register base address: 0x8A00_0180 bits 3~6 (GPIO54~51)
Analog GPIO (output only) register base address: 0x8A00_0180 bits 7~10 (GPIO58~55)

Table 42: MCU GPIO control registers (base address: 0x8A00_0000).

Address	Signal	Bit Pos	R/W	Default	Description
0x00	GPIODATA	[15:0]	R/W	0	GPIO data register
0x04	GPIODMSK	[15:0]	R/W	0	GPIO data mask register, GPIO pin can be read and written if the mask bit is “1”
0x08	GPIODIR	[15:0]	R/W	0	GPIO direction 1: configure pin to be output 0: configure pin to be input
0x0C	GPIOIS	[15:0]	R/W	0xFFFF	Interrupt sense register. 1: detect levels 0: detect edges
0x10	GPIOIBE	[15:0]	R/W	0	Interrupt both edges register. 1: both edges trigger an interrupt, 0: interrupt generation event is controlled by GPIOIEV
0x14	GPIOIEV	[15:0]	R/W	0xFFFF	Interrupt event register 1: rising edges or high levels trigger interrupts. 0: falling edges or low levels trigger interrupts.
0x18	GPIOIE	[15:0]	R/W	0	Interrupt mask register 1: corresponding pin is not masked 0: corresponding pin interrupt is masked
0x1C	GPIORIS	[15:0]	R only	0	Row interrupt status, reflect the status of interrupts trigger conditions detection on pins (prior to masking). 1: interrupt condition met 0: condition not met
0x20	GPIOMIS	[15:0]	R only	0	Masked interrupt status 1: Interrupt active 0: interrupt not active
0x24	GPIOIC	[15:0]	W only	0	Interrupt clear 1: clear edge detection interrupt 0: no effect
0x40	GPIOITCR	[0]	R/W	0	Integration test control register 1: In integration test mode 0: Normal mode

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Address	Signal	Bit Pos	R/W	Default	Description
0x44	GPIOITOP1	[15:0]	W only	0	Integration test input read/set register. In integration test mode, writes specify the value to be driven on the GPIOMIS lines. Read GPIOMIS checks interrupt active.
0x48	GPIOITOP2	[0]	W only	0	Integration test input read/set register. In integration test mode, reads return the value of GPIOINTR.

4.8.9 Auxiliary Analog-to-Digital Converter (ADC)

SC6600D provides five general-purpose ADC inputs and they can be used to monitor analog variables in the system, e.g., temperature, touch panel, and other house keeping parameters. In addition, two internal inputs are provided for battery voltage and charger program voltage measurement.

The auxiliary ADC consists of the following parts:

- Input mux, which selects one of the five analog inputs and sends it to the converter.
- A 10-bit analog-to-digital converter (ADC), which converts the analog input to a digital word.

Whenever an input is selected the ADC automatically powers up. At the end of the conversion, the ADC sends an interrupt to the MCU and then automatically powers down. The MCU then can read the digital value from the result register.

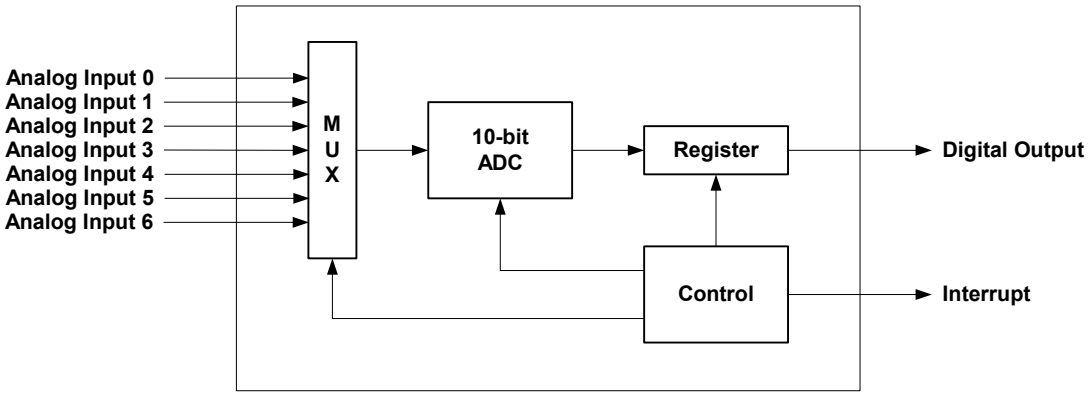

Figure 17: Auxiliary ADC.

Two different voltage ranges of analog input can be measured with the build-in resistor dividers. AUXADCS1 [4:0] corresponds to the 5-channel analog input resistor divider. AUXADCS1 [4:0] being high enables the resistor divider. Normally, with resistor divider the analog input voltage range is 3.5 V, without the resistor divider the analog input voltage range is 1.2 V.

Note:

- The input resistor divider is not available for ADC3, and therefore the analog input voltage range for ADC3 is only limited to 1.1V.

4.8.9.1 Auxiliary ADC control registers

Table 43: Auxiliary ADC control registers (base address: 0x8B00_0000).

Address	Signal	Bit Pos	R/W	Default	Description
0x0000	ADCCTL	[6:0]		0	ADC input mux control. Each bit corresponds to one input. When one bit is high, the corresponding input is selected. Only the data with all zeros or one bit one and other bits are zeros can be written into this register. If all input bits are ones, this register is set to zero.

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Address	Signal	Bit Pos	R/W	Default	Description
		[7]		0	ADC calibration bypass
		[8]		0	ADC test enable.
		[13:9]		0	AUXADCS1 [4:0]. Five channel input resistor divider enable. (Note: The divider is not available for ADC3.) 1: Enable the divider 0: Disable the divider
		[15:14]			Reserved.
0x0004	ADCR	[9:0]	R only		ADC result
		[15:10]			Reserved.

4.9 Real Time Clock

The MCU sub-system provides real time clock support.

The day counter has 16 bits and therefore can count for 65,536 days.

4.9.1 Real Timer Clock Registers

Table 44: Real time clock registers (base address: 0x8900_0000).

Address	Signal	Bit Pos	R/W	Default	Description
0x0000	Second_count	[5:0]	R only	N/A	Current second count
0x0004	Minute_count	[5:0]	R only	N/A	Current minute count
0x0008	Hour_count	[4:0]	R only	N/A	Current hour count
0x000C	Day_count	[15:0]	R only	N/A	Current hour count
0x0010	Second_update	[5:0]	W only		Write to update second count
0x0014	Minute_update	[5:0]	W only		Write to update minute count
0x0018	Hour_update	[4:0]	W only		Write to update hour count
0x001C	Day_update	[15:0]	W only		Write to update day count
0x0020	Second_alm	[5:0]	R/W	N/A	Alarm second count
0x0024	Minute_alm	[5:0]	R/W	N/A	Alarm minute count
0x0028	Hour_alm	[4:0]	R/W	N/A	Alarm hour count
0x002C	Day_alm	[15:0]	R/W	N/A	Alarm day count
0x0030	Rtc_control	[15:0]	R/W		RTC control
	Sec_ie	[0]		0	Sec interrupt enable
	Min_ie	[1]		0	Min interrupt enable
	Hour_ie	[2]		0	Hour interrupt enable
	Day_ie	[3]		0	Day interrupt enable
	Alarm_ie	[4]		0	Alarm interrupt enable
	Hour_format_sel	[5]		0	Hour format select 0: The read back hour count is formatted as 0 to 24. 1: The read back hour count is formatted as 0 to 12, and bit 4 represent AM (0) or PM (1).
0x0034	Rtc_int	[15:0]	R only		RTC interrupts
	Sec_int	[0]		0	Second interrupt
	Min_int	[1]		0	Minute interrupt
	Hour_int	[2]		0	Hour interrupt
	Day_int	[3]		0	Day interrupt
	Alm_int	[4]		0	Alarm interrupt
0x0038	Rtc_int_clr	[15:0]	W only		RTC interrupt clear
	Sec_int_clr	[0]		0	Second interrupt is cleared by writing 1 to this bit

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Address	Signal	Bit Pos	R/W	Default	Description
	Min_int_clr	[1]		0	Minute interrupt is cleared by writing 1 to this bit
	Hour_int_clr	[2]		0	Hour interrupt is cleared by writing 1 to this bit
	Day_int_clr	[3]		0	Day interrupt is cleared by writing 1 to this bit
	Alm_int_clr	[4]		0	Alarm interrupt is cleared by writing 1 to this bit
0x003C	Rtc_int_masked	[15:0]	R/W		RTC interrupt masked
	Sec_int_masked	[0]		0	
	Min_int_masked	[1]		0	
	Hour_int_masked	[2]		0	
	Day_int_masked	[3]		0	
	Alm_int_masked	[4]		0	

4.10 GEA Accelerator

4.10.1 GPRS Encryption Algorithm (GEA)

GEA algorithms are options for the GPRS channels and SC6600D supports both GEA 1 and GEA 2. The GEA accelerator is controlled by the MCU. The accelerator generates the cipher bit steam, and the MCU performs the final XOR of the bit steams.

4.10.2 GEA Accelerator Control

Table 45: GEA accelerator control registers (base address: 0x8D00_0000).

Address	Signal	Bit Pos	R/W	Default	Description
0x8D00_0000 to 0x8D00_0C7F	KEYSTREAM TABLE	[15:0]	R/W	0	3 – 1600 bytes of key stream depending on WORD_LEN
0x8D00_0C80	GEA MODE	[1:0]	R/W	0	0: Encryption Disable 1: GEA I encryption 2: GEA II encryption 3: Reserved
	Reserved	[15:2]			
0x8D00_0C84	WORD_LEN	[9:0]	R/W	0	Specify how many words (2 bytes) of key stream need to be generated. Max 800.
		[14:10]			Reserved
	DIR	[15]	R/W	0	Single bit direction
0x8D00_0C88	Kc [15:0]	[15:0]	R/W	0	First word of Kc
0x8D00_0C8C	Kc [31:16]	[15:0]	R/W	0	Second word of Kc
0x8D00_0C90	Kc [47:32]	[15:0]	R/W	0	Third word of Kc
0x8D00_0C94	Kc [63:48]	[15:0]	R/W	0	Fourth word of Kc
0x8D00_0C98	INPUT [15:0]	[15:0]	R/W	0	First word of INPUT
0x8D00_0C9C	INPUT [31:16]	[15:0]	R/W	0	Second word of INPUT
0x8D00_0CA0	GEA_START		R only		Read this location to start GEA key stream generation
0x8D00_0CA4	POLL_REG	[0]	R/W		This is the polling register, when high, indicating GEA key stream is ready. Software is responsible for clearing it after read

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4.11 MCU Global Registers

Table 46: MCU global registers (base address: 0x8B00_0000).

Address	Signal	Bit Pos	R/W	Default	Description
0x8B00_0000	ADCCTL	[15:0]	R/W		ADC control
		[6:0]		0	ADC input mux control. Each bit corresponds to one input. When one bit is high, the corresponding input is selected. Only the data with all zeros or one bit one and other bits are zeros can be written into this register. If all input bits are ones, this register is set to zero.
		[7]		0	ADC calibration bypass
		[8]		0	ADC test enable.
		[13:9]		0	AUXADCS1 [4:0]. Five channel input resistor divider enable. Note: The divider is not available on ADC3. 1: Enable the divider 0: Disable the divider
		[15:14]			Reserved.
0x8B00_0004	ADCR	[9:0]	R only		ADC result
		[15:10]			Reserved.
0x8B00_0008	GEN0	[15:0]	R/W	0	General control
		[0]		0	Wdg_en
		[1]		0	Reserved
		[2]		0	timers_eb: enable timers
		[3]		0	sim_eb: enable SIM
		[4]		0	2ws_eb: enable 2-wire serial port
		[5]		0	pwm_b_eb: enable pwm_b
		[6]		0	pwm_a_eb: enable pwm_a
		[7]		0	rtc_eb: RTC enable
		[8]		0	kpd_en: keypad enable
		[9]		0	Reserved
		[10]		0	mcu_dsp_rst, MCU reset DSP
		[11]		0	mcu_soft_rst, MCU soft reset, active high. MCU sets this bit, and after delay of 15 clocks, this bit changes to low.
		[12]		0	Mcu_pllpd_en, PLL power down enable
		[13]		0	dsp_start_0
		[14]		0	Reserved
		[15]		0	Sys_pd: system power down
0x8B00_000C	PCTL	[3:0]	R/W	pad_dsp_ctl [3:0]	clk_mcu_div [3:0]. MCU clock divisor. If clk_mcu_div = N, the MCU clock frequency is the PLL output frequency divided by (N+1).
		[7:4]	R/W	pad_dsp_ctl [7:4]	clk_dsp_div [3:0]. DSP clock divisor. If clk_dsp_div = N, the DSP clock frequency is the PLL output frequency divided by (N+1).
		[8]	R/W	~pad_dsp_ctl [8]	test_mode (testmodep). This is connected to all TeakLite related clock-gating cells. When this bit is 1, all those clock gatings are disabled.

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Address	Signal	Bit Pos	R/W	Default	Description
		[9]	R/W	~pad_dsp_ctl [9]	all_clk_en. When this bit is 1, all clock gatings are disabled.
		[10]	R/W	~pad_dsp_ctl [10]	dsp_ext_z. Enables the use of external z-space memory.
		[15:11]	R/W	~pad_dsp_ctl [15:11]	strap_bits [4:0], TeakLite strap bits. [0] = EXTP (ZD [0]), external program mode [1] = TESETP (ZD [1]), test mode [2] = BOOTP (ZD [2]), boot mode, i.e., start from address 0xFFFE [3] = DBGP (ZD [3]), debug mode [4] = URSTP (ZD [4]), user reset to OCEM
0x8B00_0010	INT	[0]	R only	0	dsp_irq: DSP sets this bit by signal dsp_irq_pls
		[1]	R only	0	dsp_frq: DSP sets this bit by signal dsp_frq_pls
		[2]	R only	0	mcu_irq: MCU sets this bit, and after delay 15 clocks, the bit changes to low
		[3]	R only	0	mcu_frq: MCU sets this bit, and after delay 15 clocks, the bit changes to low
		[4]	R only	0	adc_irq: The bit is set by signal adc_irq_pls
		[5]	R only	0	vbc_irq: The bit is set by signal vbc_dsp_int
		[7:6]			Reserved
		[8]	R only	0	mon_irq0: The bit is set by signal mon_irq0_pls
		[9]	R only	0	mon_irq1: The bit is set by signal mon_irq1_pls
		[10]	R only	0	mon_irq2: The bit is set by signal mon_irq2_pls
		[11]	R only	0	mon_irq3: The bit is set by signal mon_irq3_pls
		[12]	R only	0	mon_irq4: The bit is set by signal mon_irq4_pls
		[13]	R only	0	mon_irq5: The bit is set by signal mon_irq5_pls
		[14]	R only	0	mon_irq6: The bit is set by signal mon_irq6_pls
		[15]	R only	0	mon_irq7: The bit is set by signal mon_irq7_pls
0x8B00_0014	ICLR	[0]	W only	0	Write “1” clear DSP_irq
		[1]			Write “1” clear DSP_frq
		[3:2]			
		[4]			Write “1” clear adc_irq (internal control register)
		[5]			Write “1” clear vbc_irq (internal control register)
		[7:6]			Reserved
		[8]			Write “1” clear mon_irq0
		[9]			Write “1” clear mon_irq1
		[10]			Write “1” clear mon_irq2

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Address	Signal	Bit Pos	R/W	Default	Description
		[11]			Write “1” clear mon_irq3
		[12]			Write “1” clear mon_irq4
		[13]			Write “1” clear mon_irq5
		[14]			Write “1” clear mon_irq6
		[15]			Write “1” clear mon_irq7
0x8B00_0018	GEN1	[3:0]		0x0	CLK_DLY [3:0], MCU clock delay control for off-chip output. The nominal delay is 2 ns times the value of [2:0], and [3] inverts the clock.
		[7:4]		0x5	clk_vb_div [3:0]. VB clock divisor. If clk_vb_div = N, the VB clock frequency is the PLL output frequency divided by (N+1)*13. vb_clk default value is 1MHZ
		[8]		0	gea_eb, GEA enable
		[9]		0	pllmn_we, pll_mn register write enable
		[10]		0	Reserved
		[11]		0	rempause_eb, remap/stop register enable
		[12]		0	testmodep_mcu, gate clock disable
		[13]		0	syst_en, system timer enable
		[14]			Reserved.
		[15]		0	Reserved.
		[19:16]		0x0	mem_clk_dly: bit 3~0
		[20]	R only		Arm_boot_md0
		[21]	R only		Arm_boot_md1
		[22]		0	Serclk_eb0
		[23]		0	Serclk_eb1
		[24]		0	Serclk_eb2
		[25]		0	Dma_eb
		[29:26]		0	Dcam_clk_dly bit 3~0
		[31:30]		0	Dcam_clk_sel, select pin ARMCLK output “0” clk_mcu, “1” clk_mcu divided by 2 “2” clk_mcu divided by 4
0x8B00_001C	PCMCIA_CTL	[3:0]		0x1	CLK_PCM_DIV [3:0], clock divisor for the PCMCIA interface. If the value is N, the frequency of the PCMCIA clock is the PLL output frequency divided by (N+1).
		[4]		0	CLK_PCM_EN, enable PCMCIA interface
		[7:5]			Reserved
		[8]		0	PCM_RELEASE
		[15:9]		0	Reserved
0x8B00_0020	HWRST	[15:0]		0	The register value do not change on MCU reset, it can only be cleared by reset ext_rst_b.

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Address	Signal	Bit Pos	R/W	Default	Description
0x8B00_0024	PLL_MN	[15:0]		0x1e05	PLL frequency control [15:8] M [7:0] N PLL frequency = input frequency * M / N The MCU can change this register when GEN1[9], pllmn_we is high. N must be greater than 2.
0x8B00_0028	LDO_CTL	[0]		0	ldo_bp18. When set, VDD will be powered down (LDO bypassed).
		[1]		0	ldo_bp18_rst. When set, VDD will be powered on (LDO bypassed reset).
		[2]		0	ldo_bprf0
		[3]		0	ldo_bprf0_rst
		[4]		0	ldo_bprf1
		[5]		0	ldo_bprf1_rst
		[6]		0	ldo_bpio
		[7]		0	ldo_bpio_rst
		[8]		0	ldo_bpmem
		[9]		0	ldo_bpmem_rst
		[10]		0	ldo_vref27
		[11]		0	ldo_vref27_rst
		[12]		0	ldo_bppll
		[13]		0	ldo_bppll_rst
		[14]		0	ldo_bpvbo
		[15]		0	ldo_bpvbo_rst
		[16]		0	ldo_bpvb
		[17]		0	ldo_bpvb_rst
		[18]		0	ldo_bpd3v
		[19]		0	ldo_bpd3v_rst
		[20]		0	ldo_bpvbb
		[21]		0	ldo_bpvbb_rst
		[22]		0	ldo_bpaux
		[23]		0	ldo_bpaux_rst
		[24]		0	ldo_bpsim
		[25]		0	ldo_bpsim_rst
		[26]		0	fsm_ldorfbp_en. When set, LDO1 and LDO2 will be off in sleep mode.
		[27]		0	fsm_ldoauxbp_en. When set, AUX LDO will be off in sleep mode.
		[28]		0	fsm_ldod3vbp_en. When set, D3V LDO will be off in sleep mode.
		[29]		0	fsm_afcpd_en. When set, AFC LDO will be off in sleep mode.
		[30]		0	pdbg
		[31]		0	pdbg_rst
0x8B00_002C	GEN2	[0]		0	Arm_mem_en0
		[1]		0	Arm_mem_en1
		[2]		1	Arm_mem_en2
		[3]		1	Arm_mem_en3
		[4]		0	Arm_boot_en
		[7:5]		0	Reserved

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Address	Signal	Bit Pos	R/W	Default	Description
		[9:8]		0	Ser_sel0: Serial port 0 select “0” UART “1” IrDA “2” SPI
		[11:10]		0	Ser_sel1: “0” UART “1” IrDA “2” SPI
		[13:12]		0	Ser_sel2: “0” UART “1” IrDA “2” SPI “3” DCAM
		[14]		0	uart_mux_sel1 “0” MCU controls UART1 “1” DSP controls UART1
		[15]		1	uart_mux_sel2 “0” MCU controls UART2 “1” DSP controls UART2
		[19:16]		0x0	Gpio_eb3~0: bit0 enables gpio0~15 bit1 enables gpio16~31 bit2 enables gpio32~47 bit3 enables gpio48~58
		[31:20]			
0x8B00_0030	ARM_BOOT_ADDR	[15:0]		0x0000	arm_boot_addr
0x8B00_0034	STC_STATE	[15:0]	R only		Reserved.
0x8B00_0038	LDO_CTL2	[0]		0	ldo_core_b0
		[1]		0	ldo_core_b0_rst
		[2]		0	ldo_core_b1
		[3]		0	ldo_core_b1_rst
		[4]		0	ldo_rtc_b0
		[5]		0	ldo_rtc_b0_rst
		[6]		0	ldo_rtc_b1
		[7]		0	ldo_rtc_b1_rst
		[8]		0	ldo_sim_b0
		[9]		0	ldo_sim_b0_rst
		[10]		0	ldo_sim_b1
		[11]		0	ldo_sim_b1_rst
		[12]		0	slp_core_b0
		[13]		0	slp_core_b0_rst
		[14]		0	slp_core_b1
		[15]		0	slp_core_b1_rst
		[16]		0	ldo_pll_b0
		[17]		0	ldo_pll_b0_rst
		[18]		0	ldo_pll_b1
		[19]		0	ldo_pll_b1_rst
		[20]		0	slp_pll_b0
		[21]		0	slp_pll_b0_rst
		[22]		0	slp_pll_b1
		[23]		0	slp_pll_b1_rst
		[24]		0	fsm_xtlen_en. When set, XTLEN will be low in sleep mode.

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Address	Signal	Bit Pos	R/W	Default	Description
		[25]		0	auto_b_en. When set, another set of VDD level control (slp_core_b0/b1 at 0x8B00_0038 [15:12]) will be used in sleep mode.
		[26]		0	Slp_core_en
		[27]		0	Slp_io_en
		[28]		0	Slp_mem_en
		[29]		0	Slp_sim_en
		[30]		0	Fsm_ldopllbp_en
		[31]			Reserved
0x8B00_003C	ANATST_CTL	[0]		0	start_en1u
		[1]		0	start_en1u _rst
		[2]		0	start_en2u
		[3]		0	start_en2u _rst
		[4]		0	start_en3u
		[5]		0	start_en3u _rst
		[6]		0	Reserved
		[7]		0	Reserved
		[13:8]			
		[14]		0	Recharge
		[15]	R only		Standby
		[27:16]			
		[31:28]		0	Charger_ctl, charger control
0x8B00_0040	SYST_ALM	[31:0]		0x0000_FFFF	syst_alm
0x8B00_0044	BUSCLK_ALM	[2:0]		0	Bus_clk_dvdr bit2~0
		[3]		0	arm_vb_da0on, enable VB DAC1 digital path. This bit is active when arm_vb_acc is high.
		[4]		0	arm_vb_da1on, enable VB DAC0 digital path. This bit is active when arm_vb_acc is high.
		[5]		0	arm_vb_adcon, enable VB ADC digital path. This bit is active when arm_vb_acc is high.
		[6]		0	arm_vb_anaon, enable VB clock for analog. This bit is active when arm_vb_acc is high.
		[7]		0	arm_vb_acc, MCU voice band access enable
		[9:8]		0	dma_vbad_sel “0” dma0, 2, 4 connect to UART “1” dma0 connect to VBAD “2” dma2 connect to VBAD “3” dma4 connect to VBAD
		[13:10]			Reserved
		[14]		0	Clk_mcu_inv
		[15]		0	mcu_mn_en, MCU clock MN divisor register write enable
		[16:23]		0	Reserved
		[27:24]		0	mcu_div_m
		[31:28]		0	mcu_div_n
0x8B00_0048	Mcu_misc_en	[31:0]			
		[0]		0	Clk_mcu_out enable
		[1]		0	Clk_dsp_out enable

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Address	Signal	Bit Pos	R/W	Default	Description
		[2]		0	Spg clk_13mhz enable
		[3]		0	Spg clk_agc enable
		[4]		0	Spg clk_qbc enable
		[5]		0	Spg clk_vbc6.5 enable
		[6]		0	Spg clk_btx enable
		[7]		0	Spg clk_brx enable
		[8]		0	Spg clk_32K enable
		[9]		0	Spg clk_dsp. enable
		[10]		0	Spg clk_pcm enable
		[11]		0	Spg clk_mcu enable
		[12]		1	ARM clk_tic enable
		[13]		0	ARM clk_mon enable for bus monitor
		[30:14]			Reserved
		[31]		0	Reserved (Mcu_hpass)
0x8B00_004C	Soft_rst	[0]			Keypad_soft_rst. Write 1 to this bit reset keypad block.
		[31:1]			
0x8B00_0050	Ext_mem_dly	[29:0]			External memory signal delay controls
		[2:0]		1	Ext_addr0_dly
		[5:3]		2	Ext_addr8_dly
		[8:6]		3	Ext_addr16_dly
		[11:9]		1	Ext_data0_dly
		[14:12]		2	Ext_data8_dly
		[17:15]		2	Ext_csn0_dly
		[20:18]		2	Ext_csn1_dly
		[23:21]		2	Ext_csn2_dly
		[26:24]		2	Ext_we_dly
		[29:27]		2	Ext_bhbl_dly
		[31:30]			Reserved
0x8B00_0054	Ext_mem_dly_ cs3	[14:0]			More memory signal delay controls
		[2:0]		2	Ext_csn3_dly
		[5:3]		2	Ext_csn4_dly
		[8:6]		2	Ext_csn5_dly
		[11:9]		2	Ext_csn6_dly
		[14:12]		2	Ext_csn7_dly
		[31:15]			Resered

4.12 Chip Pin Control

4.12.1 Pin Function Selection

The control bits for pad function selections are listed in the following table. A selection value of 0 selects the 1st pin function, a value of 1 selects the 2nd function, a value of 2 selects the 3rd function and a value of 3 selects the 4th function (if applicable). Some of the functions are for test and debug purposes only and therefore not described in this document.

4.12.2 Pad Driving Strength

The Driving strength of digital I/O pads can be programmed through control registers from 2X to 10X. For a 6X driver, the maximum load is 20 pF for 50 MHz operations. There are two control bits and the setting are as follows.

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Table 47: SC6600D I/O Driving strength control.

Control Bits	Driving Strength
00	2X
01	6X
10	12X
11	24X

4.12.3 Pad Weak Pull-Up

The digital I/O pads provide a built-in weak pull-up (WPU) resister that can be activated or deactivated at the control of the MCU. When activated, the weak pull-up resistance is about 40 kΩ.

4.12.4 Chip Pin Control Registers

Table 48: Chip pin control registers (base address: 0x8C00_0000).

Address	Register	Signal	Bit Pos	Default	Description
0x8C00_0000	Sel_reg0	PA4/BOOT_sel	[9:8]	0	PWMA select: 0. XADV 1. PA4 2. U2TXD 3. ARM GPIO42
0x8C00_0008	Sel_reg2	RFCTL13_sel (PA16)	[1:0]	0	PA16 select: 0. PA RD 1. DSP Timer 1 2. RF control 13 3. ARM GPIO21
0x8C00_000C	Sel_reg3	RFCTL9_sel (PD6)	[13:12]	0	PD6 select: 0. PD 6 1. RFCTL 9 2. UART U2DTRN 3. ARM GPIO 6
0x8C00_0010	Sel_reg4	RFCTL10_sel (PD8)	[1:0]	0	PD8 select: 0. PD 8 1. RFCTL 10 2. UART U2RTSN 3. ARM GPIO 7
		RFCTL11_sel (PD9)	[3:2]	0	PD9 select: 0. PD 9 1. RFCTL 11 2. UART U2DSRN 3. ARM GPIO 8
		RFCTL12_sel (PD10)	[5:4]	0	PD10 select: 0. PD 10 1. RFCTL 12 2. UART U2CTSN 3. ARM GPIO 9
		CSN2_sel (PD12)	[9:8]	0	CSN2 select: 0. EMA CS 2 1. PD 12 2. 3. ARM GPIO 10
		CSN3_sel (PD13)	[11:10]	0	CSN3 select: 0. EMA CS 3 1. PD 13 2. 3. ARM GPIO 11

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Address	Register	Signal	Bit Pos	Default	Description
0x8C00_0014	Sel_reg5	XTLEN_sel	[1:0]	0	XTLEN select: 0. XTLEN 1. DSP ZA bit 0 (O) 2. DSP GPIO 9 3. ARM GPIO 12
		SYSPD_sel	[3:2]	0	SYSPD select: 0. SYSPD 1. DSP ZA bit 1 (O) 2. UART1 U1CSN 3 3. ARM GPIO 13
		KEYIN4/A23_sel	[5:4]	0	KEYIN4/A23 select: 0. EMA 23 1. DSP ZA bit 2 (O) 2. KEYIN 4 3. ARM GPIO 14
		PBINT_sel	[7:6]	0	PBINT select: 0. PBINT 1. DSP ZA bit 3 (O) 2. DSP GPIO 11 3. ARM GPIO 15
		GPIO26_sel	[9:8]	0	GPIO26 select: 0. MCU GPIO26 (I/O) 1. DSP ZA bit 4 (O) 2. DCAM CCIR_CLK (I) 3. VB SSRST_N (I)
		GPIO27_sel	[11:10]	0	GPIO27 select: 0. MCU GPIO27 (I/O) 1. DSP ZA bit 5 (O) 2. CCIR_VS (I) 3. VB SSCLK (O)
		SCL0_sel	[13:12]	0	SCL0 select: 0. PWM b 1. DSP ZA bit 6 (O) 2. UART2 U2RTSN 3. I2C SCL
		GPIO29_sel	[15:14]	0	GPIO29 select: 0. PWM a 1. DSP ZA bit 7 (O) 2. UART2 U2CSN 3 3. MCU GPIO29 (I/O)
0x8C00_00018	Sel_reg6	EMA22_sel	[1:0]	0	EMA22 select: 0. EMA 22 1. DSP ZA bit 8 (O) 2. UART2 U2DTRN 3. MCU GPIO30 (I/O)
		RFCTL14_sel	[5:4]	0	RFCTL14 select: 0. MCU GPIO22 (I/O) 1. Output from Zrdn (O) 2. RF control bit 14 (O) 3. VB data out SSDX (O)
		RFCTL15_sel	[7:6]	0	RFCTL15 select: 0. MCU GPIO23 (I/O) 1. Output from Zwrn (O) 2. RF control bit 15 (O) 3. VB data in SSDR (I)

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Address	Register	Signal	Bit Pos	Default	Description
0x8C00_001C	Sel_reg7	KEYOUT4_sel	[13:12]	0	KEYOUT4 select: 0. KEYOUT 4 1. DSP ZD 6 2. PCMCIA D2 3. ARM GPIO35
		KEYOUT5_sel	[15:14]	0	KEYOUT5 select: 0. KEYOUT 5 1. DSP ZD 7 2. PCMCIA D3 3. ARM GPIO36
0x8C00_0020	Sel_reg8	KEYIN2_sel	[3:2]	0	KEYIN2 select: 0. KEYIN 2 1. DSP ZD 9 2. PCMCIA D6 3.
		KEYIN3_sel	[5:4]	0	KEYIN3 select: 0. KEYIN 3 1. DSP ZD 10 2. PCMCIA D7 3. ARM GPIO37
0x8C00_00038	Sel_reg14	U0RXD_sel	[1:0]	0	UART0 RXD select: 0. UART0 RXD input (I) 1. 2. MCU GPIO25 (I/O) 3. VB DAI SSCTL1 (I)
		U0TXD_sel	[3:2]	0	UART0 TXD select: 0. UART0 txd output (I/O) 1. 2. MCU GPIO24 (I/O) 3. VB DAI SSCTL0 (I)
		U1RXD_sel	[5:4]	0	UART1 RXD select: 0. UART1 RXD input (I) 1. ARM EMA22 2. PCMCIA WE_B 3. MCU GPIO43 (I/O)
		U1TXD_sel	[7:6]	0	UART1 TXD select: 0. UART1 txd output (I/O) 1. ARM CSN2 2. PCMCIA REG_B 3. MCU GPIO44 (I/O)
		U2RXD_sel	[13:12]	0	U2RXD select: 0. I2C SCL 1. DSP GPIO 10 2. UART2 RXD input (I) 3. MCU GPIO32 (I/O)
		SDA_sel	[15:14]	0	SDA select: 0. ARM EMA24 1. I2C SDA 2. DCAM CCIR_HS 3. MCU GPIO31 (I/O)
0x8C00_003C	Sel_reg15	RFCTL0_sel	[1:0]	0	RFCTL0 select: 0. ARM CSN5 1. TEST RXID 2. RFCTL0 3. DSP GPIO 3

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Address	Register	Signal	Bit Pos	Default	Description
		RFCTL1_sel	[3:2]	0	RFCTL1 select: 0. ARM CSN6 1. TEST RXQD 2. RFCTL1 3. DSP GPIO 4
		RFCTL2_sel	[5:4]	0	RFCTL2 select: 0. RFCTL2 1. TEST VADOUT 2. 3. DSP GPIO 5
		RFCTL3_sel	[7:6]	0	RFCTL3 select: 0. ARM CSN7 1. TEST VDACD0 2. RFCTL3 3. ARM GPIO 0
		RFCTL4_sel	[9:8]	0	RFCTL4 select: 0. RFCTL4 1. TEST VDACD1 2. 3. ARM GPIO 1
		RFCTL5_sel	[11:10]	0	RFCTL5 select: 0. RFCTL5 1. TEST VBCLK13 2. 3. ARM GPIO 2
		RFCTL6_sel	[13:12]	0	RFCTL6 select: 0. RFCTL6 1. TEST VBCLKADC 2. VB DAI SSDX (O) 3. ARM GPIO 3
		RFCTL7_sel	[15:14]	0	RFCTL7 select: 0. RFCTL7 1. CKE 2. VB DAI SSDR (I) 3. ARM GPIO 4
0x8C00_0040	Sel_reg16	RFCTL8_sel	[1:0]	1 Write only	RFCTL8 select: 0. DSP GPIO 8 1. RFCTL8 2. UART0 U0CSN 3 3. ARM GPIO 5
		RFSCK_sel	[3:2]	0	RFSCK select: 0. RFSCK 1. STOP 2. 3. DSP GPIO 1
		RFSDA_sel	[5:4]	0	RFSDA select: 0. RFSDA 1. ABORT_N 2. 3. DSP GPIO 0
		RFSEN_sel	[7:6]	0	RFSEN select: 0. RFSEN 1. CONT_N 2. 3. DSP GPIO 2

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Address	Register	Signal	Bit Pos	Default	Description
		KEYOUT0_sel	[9:8]	0	KEYOUT0 select: 0. KEYOUT0 1. 2. PCMCIA CE1_B 3.
		KEYOUT1_sel	[11:10]	0	KEYOUT1 select: 0. KEYOUT1 1. 2. PCMCIA IORD_B 3.
		KEYOUT2_sel	[13:12]	0	KEYOUT2 select: 0. KEYOUT2 1. 2. PCMCIA RST 3. ARM GPIO 33
		KEYOUT3_sel	[15:14]	0	KEYOUT3 select: 0. KEYOUT3 1. 2. PCMCIA D1 3. ARM GPIO 34
0x8C00_0044	Sel_reg17	MTCK_sel	[1:0]	0	MTCK select: 0. MTCK 1. UART0 U0DSRN 2. DTCK 3. ARM GPIO 18
		MTDI_sel	[3:2]	0	MTDI select: 0. MTDI 1. UART0 U0RTSN 2. DTDI 3. ARM GPIO 17
		MTDO_sel	[5:4]	0	MTDO select: 0. MTDO 1. UART0 U0DTRN 2. DTCK 3. ARM GPIO 16
		MTMS_sel	[7:6]	0	MTMS select: 0. MTMS 1. UART0 U0CTSN 2. DTMS 3. ARM GPIO 19
		MTRST_N_sel	[9:8]	0	MTRST_N select: 0. MTRST_N 1. PWM b 2. DTINT 3. ARM GPIO 20
		KEYIN0_sel	[11:10]	0	KEYIN0 select: 0. KEYIN 0 1. DSP ZD8 2. PCMCIA D4 3.
		KEYIN1_sel	[13:12]	0	KEYIN1 select: 0. KEYIN1 1. 2. PCMCIA D5 3.
0x8C00_0048	Sel_reg18	SIMCLK_sel	[1:0]	0	SIMCLK
		SIMDA_sel	[3:2]	0	SIMDA

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Address	Register	Signal	Bit Pos	Default	Description
		CSN4_sel	[5:4]	0	EMCS[4] select: 0. EMCS[4] out 1 2 3. ARM GPIO 46
		SIMPE_sel	[7:6]	0	SIMPE
		CLKMCU_sel	[13:12]	0	CLKMCU select: 0. CLKMCU 1. CLKDSP 2. CLKPLL 3. CLK32K
0x8C00_004C	Sel_reg19	RXIN_sel	[5:4]	0	RXIN select: 0. ANALOG RXIN 1. RFCTL14 2. UART1 U1DSRN 3. DSP GPIO36 o
		RXIP_sel	[7:6]	0	RXIP select: 0. ANALOG RXIP 1. RFCTL15 2. UART1 U1CTSN 3. DSP GPIO37 o
		RXQN_sel	[9:8]	0	RXQN select: 0. ANALOG RXQN 1. RFCTL13 2. UART1 U1RTSN 3. DSP GPIO35 o
		RXQP_sel	[11:10]	0	RXQP select: 0. ANALOG RXQP 1. RFCTL8 2. UART1 U1DTRN 3. DSP GPIO34 o
		ARMCLK_sel	[13:12]	0	ARMCLK select: 0. CLKMCU 1. CLKDSP 2. CLK32K 3. ARM GPIO45
0x8C00_0064	drv_reg0	PA4/BOOT_drv	[9:8]	2	Driving strength 0~3
0x8C00_006C	drv_reg2	RFCTL13_drv (PA16)	[1:0]	0	Driving strength 0~3
		EMBH_drv	[9:8]	2	Driving strength 0~3
		EMBL_drv	[11:10]	2	Driving strength 0~3
		EMCS_N0_drv	[13:12]	2	Driving strength 0~3
		EMCS_N1_drv	[15:14]	2	Driving strength 0~3
0x8C00_0070	drv_reg3	RFCTL9_drv (PD6)	[13:12]	0	Driving strength 0~3
0x8C00_0074	drv_reg4	RFCTL10_drv (PD8)	[1:0]	0	Driving strength 0~3
		RFCTL11_drv (PD9)	[3:2]	0	Driving strength 0~3

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Address	Register	Signal	Bit Pos	Default	Description
		RFCTL12_drv (PD10)	[5:4]	0	Driving strength 0~3
		CSN2_drv (PD12)	[9:8]	2	Driving strength 0~3
		CSN3_drv (PD13)	[11:10]	2	Driving strength 0~3
0x8C00_0078	drv_reg5	XTLEN_drv	[1:0]	0	Driving strength 0~3
		SYSPD_drv	[3:2]	0	Driving strength 0~3
		KEYIN4/A23_drv	[5:4]	0	Driving strength 0~3
		PBINT_drv	[7:6]	2	Driving strength 0~3
		GPIO26_drv	[9:8]	0	Driving strength 0~3
		GPIO27_drv	[11:10]	0	Driving strength 0~3
		GPIO28_drv	[9:8]	0	Driving strength 0~3
		GPIO29_drv	[11:10]	0	Driving strength 0~3
0x8C00_007C	drv_reg6	EMA22_drv	[1:0]	2	Driving strength 0~3
		RFCTL14_drv	[5:4]	0	Driving strength 0~3
		RFCTL15_drv	[7:6]	0	Driving strength 0~3
0x8C00_0080	drv_reg7	KEYOUT4_drv	[13:12]	0	Driving strength 0~3
		KEYOUT5_drv	[15:14]	0	Driving strength 0~3
0x8C00_0084	drv_reg8	KEYIN2_drv	[3:2]	0	Driving strength 0~3
		KEYIN3_drv	[5:4]	0	Driving strength 0~3
0x8C00_0088	drv_reg9	EMA0_drv	[1:0]	2	Driving strength 0~3
		EMA1_drv	[3:2]	2	Driving strength 0~3
		EMA2_drv	[5:4]	2	Driving strength 0~3
		EMA3_drv	[7:6]	2	Driving strength 0~3
		EMA4_drv	[9:8]	2	Driving strength 0~3
		EMA5_drv	[11:10]	2	Driving strength 0~3
		EMA6_drv	[13:12]	2	Driving strength 0~3
		EMA7_drv	[15:14]	2	Driving strength 0~3
0x8C00_008C	drv_reg10	EMA8_drv	[1:0]	2	Driving strength 0~3
		EMA9_drv	[3:2]	2	Driving strength 0~3
		EMA10_drv	[5:4]	2	Driving strength 0~3
		EMA11_drv	[7:6]	2	Driving strength 0~3
		EMA12_drv	[9:8]	2	Driving strength 0~3
		EMA13_drv	[11:10]	2	Driving strength 0~3
		EMA14_drv	[13:12]	2	Driving strength 0~3
		EMA15_drv	[15:14]	2	Driving strength 0~3
0x8C00_0090	drv_reg11	EMA16_drv	[1:0]	2	Driving strength 0~3
		EMA17_drv	[3:2]	2	Driving strength 0~3
		EMA18_drv	[5:4]	2	Driving strength 0~3
		EMA19_drv	[7:6]	2	Driving strength 0~3
		EMA20_drv	[9:8]	2	Driving strength 0~3
		EMA21_drv	[11:10]	2	Driving strength 0~3
		EMOE_N_drv	[13:12]	2	Driving strength 0~3
		EMWE_N_drv	[15:14]	2	Driving strength 0~3
0x8C00_0094	drv_reg12	EMD0_drv	[1:0]	2	Driving strength 0~3
		EMD1_drv	[3:2]	2	Driving strength 0~3
		EMD2_drv	[5:4]	2	Driving strength 0~3
		EMD3_drv	[7:6]	2	Driving strength 0~3
		EMD4_drv	[9:8]	2	Driving strength 0~3
		EMD5_drv	[11:10]	2	Driving strength 0~3
		EMD6_drv	[13:12]	2	Driving strength 0~3
		EMD7_drv	[15:14]	2	Driving strength 0~3
0x8C00_0098	drv_reg13	EMD8_drv	[1:0]	2	Driving strength 0~3
		EMD9_drv	[3:2]	2	Driving strength 0~3

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Address	Register	Signal	Bit Pos	Default	Description
		EMD10_drv	[5:4]	2	Driving strength 0~3
		EMD11_drv	[7:6]	2	Driving strength 0~3
		EMD12_drv	[9:8]	2	Driving strength 0~3
		EMD13_drv	[11:10]	2	Driving strength 0~3
		EMD14_drv	[13:12]	2	Driving strength 0~3
		EMD15_drv	[15:14]	2	Driving strength 0~3
0x8C00_009C	drv_reg14	U0RXD_drv	[1:0]	0	Driving strength 0~3
		U0TXD_drv	[3:2]	0	Driving strength 0~3
		U1RXD_drv	[5:4]	0	Driving strength 0~3
		U1TXD_drv	[7:6]	0	Driving strength 0~3
		U2RXD_drv	[13:12]	0	Driving strength 0~3
		SDA_drv	[15:14]	2	Driving strength 0~3
0x8C00_00A0	drv_reg15	RFCTL0_drv	[1:0]	2	Driving strength 0~3
		RFCTL1_drv	[3:2]	2	Driving strength 0~3
		RFCTL2_drv	[5:4]	0	Driving strength 0~3
		RFCTL3_drv	[7:6]	2	Driving strength 0~3
		RFCTL4_drv	[9:8]	0	Driving strength 0~3
		RFCTL5_drv	[11:10]	0	Driving strength 0~3
		RFCTL6_drv	[13:12]	0	Driving strength 0~3
		RFCTL7_drv	[15:14]	0	Driving strength 0~3
0x8C00_00A4	drv_reg16	RFCTL8_drv	[1:0]	0	Driving strength 0~3
		RFSCK_drv	[3:2]	0	Driving strength 0~3
		RFSDA_drv	[5:4]	0	Driving strength 0~3
		RFSEN_drv	[7:6]	0	Driving strength 0~3
		KEYOUT0_drv	[9:8]	0	Driving strength 0~3
		KEYOUT1_drv	[11:10]	0	Driving strength 0~3
		KEYOUT2_drv	[13:12]	0	Driving strength 0~3
		KEYOUT3_drv	[15:14]	0	Driving strength 0~3
0x8C00_00A8	drv_reg17	MTCK_drv	[1:0]	0	Driving strength 0~3
		MTDI_drv	[3:2]	0	Driving strength 0~3
		MTDO_drv	[5:4]	0	Driving strength 0~3
		MTMS_drv	[7:6]	0	Driving strength 0~3
		MTRST_N_drv	[9:8]	0	Driving strength 0~3
		KEYIN0_drv	[11:10]	0	Driving strength 0~3
		KEYIN1_drv	[13:12]	0	Driving strength 0~3
0x8C00_00AC	drv_reg18	SIMCLK_drv	[1:0]	0	Driving strength 0~3
		SIMDA_drv	[3:2]	0	Driving strength 0~3
		CSN4_drv	[5:4]	2	Driving strength 0~3
		SIMPE_drv	[7:6]	0	Driving strength 0~3
		CLKMCU_drv	[13:12]	0	Driving strength 0~3
0x8C00_00B0	drv_reg19	ARMCLK_drv	[5:4]	0	Driving strength 0~3
0x8C00_00C8	Wpu_reg0	PA4/BOOT_wpu	[4]	0	“1” weak pull up
0x8C00_00CC	Wpu_reg1	RFCTL13_wpu (PA16)	[0]	0	“1” weak pull up
		EMA16_wpu	[4]	0	“1” weak pull up
		EMA17_wpu	[5]	0	“1” weak pull up
		EMA18_wpu	[6]	0	“1” weak pull up
		EMA19_wpu	[7]	0	“1” weak pull up
		EMA20_wpu	[8]	0	“1” weak pull up
		EMA21_wpu	[9]	0	“1” weak pull up
		EMOE_N_wpu	[10]	0	“1” weak pull up
		EMWE_N_wpu	[11]	0	“1” weak pull up

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Address	Register	Signal	Bit Pos	Default	Description
		EMBH_wpu	[12]	0	“1” weak pull up
		EMBL_wpu	[13]	0	“1” weak pull up
		EMCS_N0_wpu	[14]	0	“1” weak pull up
		EMCS_N1_wpu	[15]	0	“1” weak pull up
0x8C00_00D0	Wpu_reg2	RFCTL9_wpu (PD6)	[6]	0	“1” weak pull up
		RFCTL10_wpu (PD8)	[8]	0	“1” weak pull up
		RFCTL11_wpu (PD9)	[9]	0	“1” weak pull up
		RFCTL12_wpu (PD10)	[10]	0	“1” weak pull up
		CSN2_wpu (PD12)	[12]	0	“1” weak pull up
		CSN3_wpu (PD13)	[13]	0	“1” weak pull up
0x8C00_00D4	Wpu_reg3	XTLEN_wpu	[0]	0	“1” weak pull up
		SYSPD_wpu	[1]	0	“1” weak pull up
		KEYIN4/A23_wpu	[2]	0	“1” weak pull up
		PBINT_wpd	[3]	0	“1” weak pull down
		GPIO26_wpu	[4]	0	“1” weak pull up
		GPIO27_wpu	[5]	0	“1” weak pull up
		SCL0_wpu	[6]	0	“1” weak pull up
		GPIO29_wpu	[7]	0	“1” weak pull up
		EMA22_wpu	[8]	0	“1” weak pull up
		RFCTL14_wpu	[10]	0	“1” weak pull up
		RFCTL15_wpu	[11]	0	“1” weak pull up
0x8C00_00D8	Wpu_reg4	KEYOUT4_wpu	[6]	0	“1” weak pull up
		KEYOUT5_wpu	[7]	0	“1” weak pull up
		KEYIN2_wpu	[9]	1	“1” weak pull up
		KEYIN3_wpu	[10]	1	“1” weak pull up
0x8C00_00DC	Wpu_reg5	EMA0_wpu	[0]	0	“1” weak pull up
		EMA1_wpu	[1]	0	“1” weak pull up
		EMA2_wpu	[2]	0	“1” weak pull up
		EMA3_wpu	[3]	0	“1” weak pull up
		EMA4_wpu	[4]	0	“1” weak pull up
		EMA5_wpu	[5]	0	“1” weak pull up
		EMA6_wpu	[6]	0	“1” weak pull up
		EMA7_wpu	[7]	0	“1” weak pull up
		EMA8_wpu	[8]	0	“1” weak pull up
		EMA9_wpu	[9]	0	“1” weak pull up
		EMA10_wpu	[10]	0	“1” weak pull up
		EMA11_wpu	[11]	0	“1” weak pull up
		EMA12_wpu	[12]	0	“1” weak pull up
		EMA13_wpu	[13]	0	“1” weak pull up
		EMA14_wpu	[14]	0	“1” weak pull up
		EMA15_wpu	[15]	0	“1” weak pull up
0x8C00_00E0	Wpu_reg6	EMD0_wpd	[0]	0	“1” weak pull down
		EMD1_wpd	[1]	0	“1” weak pull down
		EMD2_wpd	[2]	0	“1” weak pull down
		EMD3_wpd	[3]	0	“1” weak pull down
		EMD4_wpd	[4]	0	“1” weak pull down

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Address	Register	Signal	Bit Pos	Default	Description
			[5]		reserve
		EMD6_wpd	[6]	0	“1” weak pull down
		EMD7_wpd	[7]	0	“1” weak pull down
		EMD8_wpd	[8]	0	“1” weak pull down
		EMD9_wpd	[9]	0	“1” weak pull down
		EMD10_wpd	[10]	0	“1” weak pull down
		EMD11_wpu	[11]	0	“1” weak pull down
		EMD12_wpu	[12]	0	“1” weak pull down
		EMD13_wpd	[13]	0	“1” weak pull down
		EMD14_wpd	[14]	0	“1” weak pull down
		EMD15_wpd	[15]	0	“1” weak pull down
0x8C00_00E4	Wpu_reg7	U0RXD_wpu	[0]	0	“1” weak pull up
		U0TXD_wpu	[1]	0	“1” weak pull up
		U1RXD_wpu	[2]	0	“1” weak pull up
		U1TXD_wpu	[3]	0	“1” weak pull up
		U2RXD_wpu	[6]	1	“1” weak pull up
		SDA_wpu	[7]	0	“1” weak pull up
		RFCTL0_wpu	[8]	0	“1” weak pull up
		RFCTL1_wpu	[9]	0	“1” weak pull up
		RFCTL2_wpu	[10]	0	“1” weak pull up
		RFCTL3_wpu	[11]	0	“1” weak pull up
		RFCTL4_wpu	[12]	0	“1” weak pull up
		RFCTL5_wpu	[13]	0	“1” weak pull up
		RFCTL6_wpu	[14]	0	“1” weak pull up
		RFCTL7_wpu	[15]	0	“1” weak pull up
0x8C00_00E8	Wpu_reg8	RFCTL8_wpu	[0]	0	“1” weak pull up
		RFSCK_wpu	[1]	0	“1” weak pull up
		RFSDA_wpu	[2]	0	“1” weak pull up
		RFSEN_wpu	[3]	0	“1” weak pull up
		KEYOUT0_wpu	[4]	0	“1” weak pull up
		KEYOUT1_wpu	[5]	0	“1” weak pull up
		KEYOUT2_wpu	[6]	0	“1” weak pull up
		KEYOUT3_wpu	[7]	0	“1” weak pull up
		MTCK_wpu	[8]	0	“1” weak pull up
		MTDI_wpu	[9]	0	“1” weak pull up
		MTDO_wpu	[10]	0	“1” weak pull up
		MTMS_wpu	[11]	0	“1” weak pull up
		MTRST_N_wpu	[12]	0	“1” weak pull up
		KEYIN0_wpu	[13]	1	“1” weak pull up
		KEYIN1_wpu	[14]	1	“1” weak pull up
0x8C00_00EC	Wpu_reg9	SIMCLK_wpu	[0]	0	“1” weak pull up
		SIMDA_wpu	[1]	0	“1” weak pull up
		CSN4_wpu	[2]	0	“1” weak pull up
		SIMRST_wpu	[3]	0	“1” weak pull up
		CLKMCU_wpu	[4]	0	“1” weak pull up
		ARMCLK_wpu	[9]	0	“1” weak pull up
		EMD5_wpd	[15]	0	“1” weak pull down
0x8C00_00F8	Ctl_reg0	PZ_sel	[2:0]	0	PD input for 000: Program Data 001: Z Bus Data 100: Z Bus Data from 208 pin
			[3]	0	Reserved
		Pin180_sel	[4]	0	Pin180_sel
		Pin208_sel	[5]	0	Pin208_sel

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Address	Register	Signal	Bit Pos	Default	Description
		Keyin4_pin_sel	[6]	0	"0" KEYIN4/A23 function 3 works as KEYIN4 input "1" use KEYIN4 as key input
			[15:7]		Reserved

4.13 Chip ID Register

Table 49: Chip ID register (base address: 0xFFFF_FFFC).

Address	Signal	Bit Pos	R/W	Default	Description
0xFFFF_FFFC	Chip ID	[31:0]	R only	0x6600_D002	Read this address will return the chip ID.

4.14 JTAG Interface

The JTAG interface can be used either by the MCU or by the DSP. The power-on default setting is for the MCU. The MCU can then write a control register to switch the JTAG interface to the DSP side.

The JTAG interface consists of the following pins.

- MTDO, test data output.
- MTDI, test data input.
- MTCK, test clock.
- MTMS, test mode.
- MTRST_N, test reset, active low. When used on the DSP side, it functions as DTINT, or test interrupt.

When not used for JTAG, these pins can be used for UART 0 hardware flow control or as GPIO pins.

4.15 Charger Control

SC6600D provides an integrated Li-ion battery charger control module. With an external PMOS transistor and a current sensing resistor, SC6600D can control the charging of Li-ion batteries.

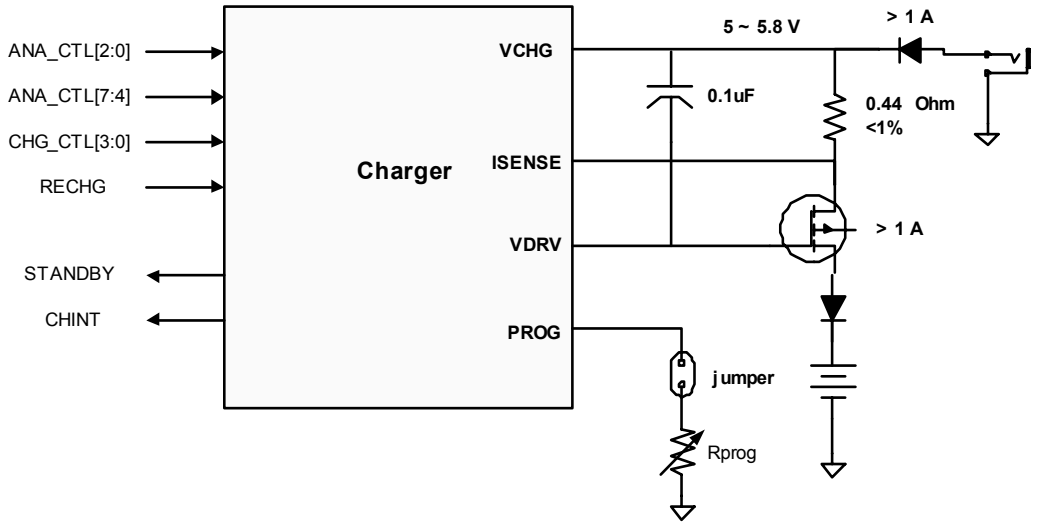

Figure 18: SC6600D charger connection.

4.15.1 Monitor of Charging Current and Battery Voltage

SC6600D can monitor both the charging current and the battery voltage with the auxiliary ADC.

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4.15.2 Charging Current

The default charging current is set at 500 mA (with no resistor connected to the PROG pin). If a larger current level is needed, an external resistor should be placed at the VPROG pin to ground, and the resistance value should be calculated as follows.

Ichg = 1.5*468/(Rint//Rext), Rint=1.5kohm

Where the current desired is in mA and R is the resistance in kΩ.

4.15.3 Recharge Control

If the charger power supply is connected, the SW can control for recharge after the initial charge is finished. The charger control circuit sends out a signal STANDBY, when the initial charge is done. The charger control circuit accepts a control signal, RECHG, with an initial value of 0. The SW can generate an active-high pulse at RECHG when the following conditions are met.

- CHINT = 1, indicating the charger power supply is connected and its voltage is > 4.8 V.
- STANDBY = 1, indicating the initial charge is done.
- VBAT is less than some predetermined value for recharge.

4.15.4 Charger Control Registers

The following table shows the control registers related to the charger, including the GPIO mapping. The GPIO settings are listed in Section 4.8.8.1.

Table 50: Charger control registers (base address: 0x8A00_0180).

Address	Signal	Bit	R/W	Default	Description
0x8B00_0000	Vprog Sel	[5]	R/W	0	This bit enables the ADC for measuring Vprog.
	Vbat Sel	[6]	R/W	0	This bit enables the ADC for measuring Vbat.
0x8B00_0004	ADC result	[9:0]	R only	-	ADC result
0x8B00_002C	GPIO EN	[19]	R/W	0	Enable for GPIO 48 ~ 58.
0x8A00_0180	GPIO 50	[2]	R only		Charger interrupt, CHINT
0x8A00_0180	GPIO 54 ~ 51	[6:3]	R only		Reserved.
0x8A00_0180	GPIO 56 ~ 55	[8:7]	W only	0	Charger termination voltage 2'b00 is the lowest, and 2'b11 is the highest.
0x8A00_0180	GPIO 57	[9]	W only	0	Charger shut down. Writing 1 to this bit will stop the charger.
0x8A00_0184	GPIOMSK	[10:7]	R/W	0	Set the mask bits to 4'b1111 to enable the corresponding control registers for GPIO55 ~ GPIO58.
		[2]	R/W	0	Charge GPIO interrupt enable bit.
0x8A00_0188	GPIODIR	[10:7]	R/W	0	Set the direction bits to 4'b1111 to use GPIO55 ~ GPIO58 as output.
0x8B00_003C	CHGCTL	[31:28]	R/W	0	Charger control [3:0]. Program bits for constant-voltage loop.
		[29:28]		0	These two bits increase the switch-point voltage. 2'b11 sets the highest voltage.
		[31:30]		0	Set the lowest switchover point between constant-current and constant-voltage modes. These two bits decrease the switch-point voltage. 2'b11 sets the lowest voltage.
0x8B00_003C	RECHG	[14]	R/W	0	Recharge control bit. Set this bit to "1" to restart the charger.

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Address	Signal	Bit	R/W	Default	Description
0x8B00_003C	STANDBY	[15]	R only	-	This bit indicates the charger status. If it is “1”, the charge is done.
0x8700_0018	Charger_int	[2]	R only	0	This bit directly reflects the charger_int input value. Charger interrupt comes from analog circuit.

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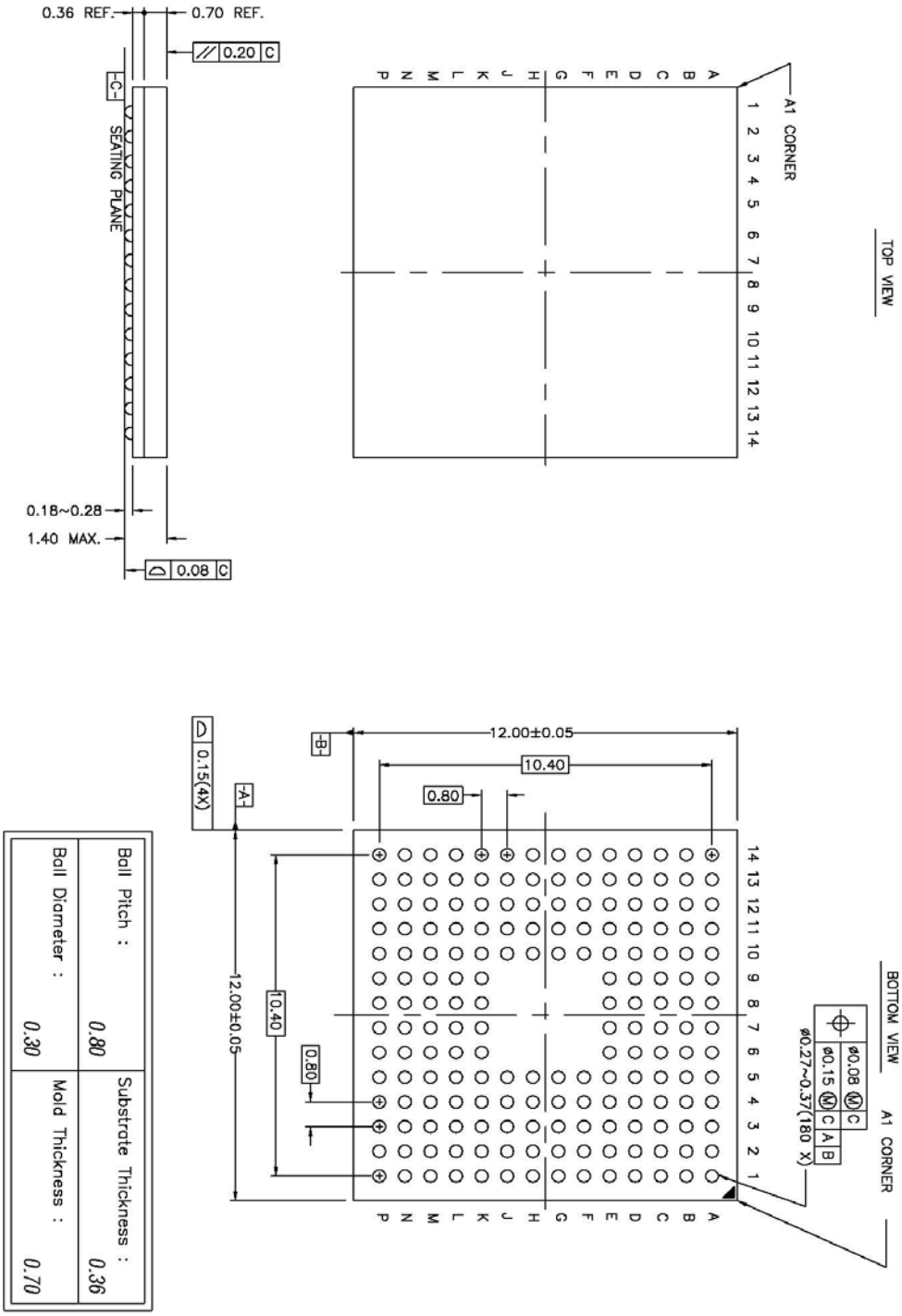
5 Package Outline



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